August, 2009

Automotive Powertrain and Body New Product Introduction (NPI)

Munir Bannoura
Agenda

► Freescale Overview, Vision, Trends and Quality
► Why Freescale for Powertrain?
► Powertrain Performance
► Technology Roadmap
► Powertrain Overview & Roadmaps
► Addressing Powertrain Customer Challenges
► Summary and Q&A
Company Overview

- Semiconductor design and manufacturing company established in 1953
- $5.2 billion in revenue in 2008
- Chairman of the Board and CEO: Rich Beyer
- Headquartered in Austin, Texas
- 24,000 employees in more than 20 countries
- 30+ years experience in automotive
- Invest over $1 billion annually on R&D
- IP portfolio contains more than 6,200 patent families
- Engaged with 10,000+ customers globally
- Offer comprehensive design solutions, including:
  - Development tools
  - Application support
  - Training
  - Documentation
  - Platforms
Our Vision, Mission and Message

Freescale Automotive provides enabling technologies that drive next-generation solutions for safer, more fuel-efficient and environmentally friendly vehicles.

This is made possible through three core principles:

1. Our leadership in driving innovative technologies for automotive applications
2. Our continued efforts to deliver high quality products through quality-driven processes
3. Our desire to build the trust of our customers through “Customer First” initiatives
Leadership

► Leader of embedded processors in the automotive industry
► Founding member of the FlexRay™ Consortium and primary silicon developer of FlexRay communications protocol
► Founding member of the Local Interconnect Network (LIN) Consortium
► Forged strategic partnerships (ST Micro and Elmos) to proliferate Freescale technology
► First semiconductor supplier to join and drive the AUTOSAR development partnership
► In 2005, opened an automotive Quality and Test Center in Nagoya, Japan—the first foreign semiconductor manufacturer to have an automotive quality and test center in the area
► Offers highest quality of automotive qualified nonvolatile memory systems
► Has a broad offering of 32-bit embedded processors built on Power Architecture™ technology
  • Software and hardware compatibility from low- to high-end
  • Scalability among different core versions and product features
  • Builds upon embedded flash experience implemented in a high density floating-gate technology
  • Unmatched efficiency—parallel processing in conjunction with sophisticated peripheral sets
  • Leverages Power Architecture tools and software ecosystem
Trust

► **Customer focus teams** (CFT): unifies company-wide divisions to handle customer programs known as “Customer First” programs

► Customer program management: assures **safe launches** via post design win support—from design win through production ramp phase

► **Field technical expertise** (FAEs and GTM): customer accessible experts to offer hands-on assistance

► Multiple fabs: spreads supply risk across multiple factories

► Multiple sourcing through **Joint Development Program** (JDP): assures best of breed products from Freescale and ST Microelectronics

► Committed to automotive: **more than 200 product families** with over 2,000 different configurations (speed, temperature, package, Pbfree vs. SnPb, and shipping method)
Automotive Electronic System Trends

Going Green

• Stringent emissions regulation
• Electronics replacing hydraulics
• Hybrids, gasoline direct injection

Safety

• Active safety systems proliferating
• Intelligence driving performance
• Higher standards of reliability required

Connectivity/Infotainment

• “Standard” convenience features
• Wireless inside and out
• Telematics/eCall systems

The Affordable Vehicle

• 30M cars in emerging markets by 2009
• Ultra-low-cost vehicles
Quality

► Freescale Quality Dashboard
  • New Product Launch ppm
  • Overall portfolio ppm
  • Incident Resolution Cycle time
  • Yield

► CEO Quality Review
  • Drive accountability for Quality metrics from top management monthly

► Customer Loyalty Survey Process
  • Drive actions for targeted improvements from customer yearly feedback

► Customer Scorecard Review Process
  • Drive actions for targeted improvements from customer monthly feedback

► Zero Defect Initiative Review
  • Drive actions for targeted minimum zero defect initiative requirements
Microcontroller Zero Defects Strategy

1. MPC500
2. S12
3. MPC5500
4. C90

NPI Quality - Cycles of Learning

Zero Defects Foundation

Defect Detection
- BIST, SCAN

Zero Defects Foundation

Design for Manufacturability
- Enhanced design rules
- Line spreading

Design for Functionality
- State of art verification/validation
- Design for Test
  - AC/DC SCAN, ATPG, IDDQ
- Partnership “Launch”

Zero Defects Foundation

4th Cycle of Zero Defect Learning
- Enhanced tools and processes improve maturity of our DFx capabilities.
- Design for Test
- Design for Manufacturability
- Design for Functionality
- Design for Failure analysis

C90
- 2008 Design
- <1 ppm Capability
Improving Freescale legacy products ppm:

- Leverage newest Design for Zero Defect methodologies, when feasible
- Apply lessons learned from customer returns on product/product families
- Apply lessons learned from Best Practices shared across the factories
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Why Freescale for Powertrain?

**lowest system cost**
- Remove knock chip, ADC muxs, temperature sensor and Vreg from PCB
- Create other “virtual sensors” using Freescale on-chip signal processing IP
- development of 90nm technology
- investigating 65nm technology

**commitment to zero defect**
- state of the art design techniques used
  - DFM, DFT, scan test
- same design rules on 16bit MCU family – 0.4ppm
- Power Architecture - 1st 1Mu with zero defects
  - currently running about 3ppm, with volume production < 1ppm

**core / system performance**
- 660DMIPS at 264MHz
- EEMBC up to 225 Automarks / 264MHz

<table>
<thead>
<tr>
<th>Compiler Target</th>
<th>mpc5554 Copperhead</th>
<th>mpc5554 BookEnd</th>
<th>mpc5554 Amroth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhrystone-2.1</td>
<td>1.00</td>
<td>1.02</td>
<td>1.00</td>
</tr>
<tr>
<td>EEMBC-automotive-1.1</td>
<td>1.00</td>
<td>1.02</td>
<td>1.00</td>
</tr>
<tr>
<td>EEMBC-consumer-1.1</td>
<td>1.00</td>
<td>1.02</td>
<td>1.00</td>
</tr>
<tr>
<td>EEMBC-networking-1.1</td>
<td>1.00</td>
<td>1.02</td>
<td>1.00</td>
</tr>
<tr>
<td>EEMBC-office-1.1</td>
<td>1.00</td>
<td>1.02</td>
<td>1.00</td>
</tr>
</tbody>
</table>

**faster time to market**
- development reuse, dual-source flexibility
- Software porting support
- software enablement package
- most complete portfolio in the industry

**Powertrain Automotive Platform**

same instruction set / memory map / interrupt map / software

- BRICs
- 4-6cyl
- diesel
- GDi
- HCCI

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Joint Development Program

► Share 32-bit Power Architecture and High Voltage PowerMOS and IGBT technologies

► Create a common Power Architecture microcontrollers design center

► Align e-NVM Process-technology on 90nm & 65nm nodes

► Collaboration between ST and FSL will compliment each companies ongoing independent roadmaps

► Devices will be jointly defined and designed, then independently manufactured, sold and supported
Freescale - ST Joint Development Program Benefits

- Two leaders of automotive MCU technologies joining forces
- True dual sourcing
- Broader IP Portfolio
- Rapidly Expanding Roadmaps
- Standardization of Power Architecture
Cross Family Compatibility

Phoenix
(Powertrain)

System Integration
Crossbar Masters
Debug
VReg
Oscillator
PowerPCTM
FMPLL
Nexus

Monaco
(Airbag/Steering)

System Integration
Crossbar Masters
Debug
VReg
Oscillator
PowerPCTM
FMPLL
Nexus

Pictus/Tokay
(Body)

System Integration
Crossbar Masters
Debug
VReg
Oscillator
PowerPCTM
FMPLL
Nexus

Bolero
(Instrument Cluster)

System Integration
Crossbar Masters
Debug
VReg
Oscillator
PowerPCTM
FMPLL
Nexus

Spectrum

System Integration
Crossbar Masters
Debug
VReg
Oscillator
PowerPCTM
FMPLL
Nexus

32-bit standard architecture adopted across all product families

- Maximum IP reuse
- Faster time-to-market
- Reduced risk
- Leverage software and tools investments
Powertrain Application Range

Market segments are all **going green** to maximize the energy conversion yield from fossil or renewable energy sources and comply with regulations applicable for a safe and fun vehicle.

- **Motorcycles & Non Auto**
  - 1 cyl Gasoline for motorbikes up to 250cc
  - 1-2 Cyl Over 250cc
  - Scooter / Skidoos / Non Automotive Engines

- **Low End Powertrain**
  - 2-4 cyl Gasoline MPI Euro3/4
  - <1,6 liter Euro4/5 Gasoline
  - Flexfuel Engines

- **High End Powertrain**
  - 4 to 12 Cylinder GDI
  - Common Rail Diesel
  - Trucks
  - Dual Clutch Transmission

- **Advanced Powertrain**
  - Hybrid Engine
  - Energy Management
  - Electrical Vehicle
  - Hydrogen Fuel Cells
  - HCCI

System in Package
Integrated solution (16 or 32-bit MCU + U-Chip) + BAP sensor

Low end 32-Bit MCU up to 1.5MB + Analog Chipset + BAP sensor

From 2MB up to Dual core 6MB MCU + (Analog Chipset + BAP Sensor)

Combination of 32-bit MCUs + Analog Chipset + cooling
32-Bit Powertrain Overview

same instruction set / memory map / interrupt map / software

- **z3**
  - BRIC
  - 2-4cyl
  - @64MHz, 512KB

- **z3**
  - @80Mz, 1.5MB

- **z4**
  - Diesel Gearbox
  - @150Mz, 2 & 4MB

- **z7**
  - GDI, Diesel
  - @264MHz, 4MB

- **2 x z7**
  - Multi-core (New)

### Time to market reduced
- Modular cores to match engine requirements
  - w/ DSP, FPU, cache, larger pre-fetch buffers
  - w/ Single and Dual-Core options
- Software enablement package
- Maximize Development reuse

### Commitment to Zero defect
- State of the art design techniques used
- Design rules applicable from S12(X) and eSys
- Proven safe launch plan

### Development Cost and Resource reduction (economies of scale)
- Common architecture and platform development
- Key IPs implementation to lower system cost as such as decimation filter, reaction channel and knock detection
- Same core & tools from BRICs to GDI engines

### Performance
- Highest performance MCU for engine management with more than 600 DMIPS benchmark at 264 MHz
- Handle regulation compliancy
- High temperature capability up to Tj=150°C
Why Power Architecture?

► Pricing and system cost
  • Market leading pricing with 130nm qualified parts
  • Development cost reduction through scalability and re-use
  • Future-proofed cost reduction with 90nm and 65nm

► Differentiation and technical strength
  • Peripherals designed specifically for engines (eTPU2 & DECFIL)
  • Performance: up to 300MHz dual core with co-processors
  • Scalability: 256k – 8MB Flash, 1 instruction set

► Quality, support and safe launch
  • Safe launch process
  • Excellent MPC5500 130nm launch, zero defect
  • Continuous improvement philosophy for 90nm
Power Architecture, More Than Just MHz

► Greatest throughput / MHz of any powertrain MCU
  • Mamba has 623 DMIPS at 264MHz (2.4 DMIPS / MHz)
  • Other similar class devices offer 1 – 1.5 DMIPS / MHz

► More than just DMIPS
  • Mamba has multiple enhanced eTPU2 modules which run faster than eTPU (200MHz vs. 132MHz)
    ▪ Each eTPU can deliver up to 1MIP/MHz in C90, CPU offers 1.5MIPS/MHz
  • Parallel processing: smart DMA, crossbar architecture and cache
  • Advanced fetch accelerator, virtual single cycle flash up to 264MHz

► Combined CPU, optimised architecture and smart peripherals
  • Gives greatest throughput, system level performance
  • Offload tasks, run slower, reduce power
  • Opportunity for ctms to add value via sw
    ▪ eTPU2 as smart watchdog
    ▪ eTPU2 running transmission module
Changes

100% compatible with eTPU
- No changes required to hardware or software if only eTPU features are used.

Supports a wider range to frequencies
- Supports up to 200MHz operation and better resolution at lower frequencies.

New channel features
- Main change is programmable channel modes.

New programming features
- Biggest change is engine relative addressing mode.

Safety related enhancements
- New software watchdog and error detection features.

Some devices have enhanced motor control features
- This is not a change to the eTPU itself but a change in integration.
- More eTPU channels have separate input and output signals to allow an eTPU to control 4 BLDC motors.
eTPU2: Engine Partitioning and Innovation

► eTPU2: more than just angle clocking

► eTPU2 example1: traction control assist
  • message from braking system & initiates torque reduction mode
  • cyclically stops fuelling & sparking selected cylinders
  • innovative traction control

► eTPU2 example2: transmission control
  • CPU & eTPU0 control engine
  • eTPU1 controls transmission
  • enables system cost reduction

► eTPU2 example3: system monitor
  • eTPU MAC unit allows for DSP filters
  • reads signals from a rotating fan
  • can indicate system wear / instability
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Performance Roadmap

36x more performance: Cerberus to Cobra

cpu32, Silver Oak, Taipan, one-at-200MHz, Mamba 264-300MHz, Cobra-dual-at-200MHz

1.2x performance
MPC5554 Copperhead
2M Flash, 64 KB SRAM
128MHz

1.5x performance
MPC5566 Viper
3M Flash, 128 KB SRAM
144MHz

2x performance
MPC56xx Mamba
4M Flash, 256 KB SRAM
264MHz

3x performance
MPC56xx Cobra
4M Flash, 256 KB SRAM
2x 180MHz

dual core, 3 eTPU, 3x perf Copperhead

single core, 2 eTPU, 2x perf Copperhead

In Production
Available
Planned
Proposed

highest ever EEMBC results, 114

benchmarked as 200MIPS

• Fully compatible products
• Dedicated automotive peripherals
• Single and dual-core options
• Covers performance needs to 2020
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Technology
### Embedded NVM Technology Roadmap

<table>
<thead>
<tr>
<th>2005+</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Industrial, Mass Market and Low End Automotive: 1.5T Split Gate Solutions</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>0.25μm Split Gate Flash</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.18μm Split Gate Flash</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90nm Split Gate Flash (TFS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>Mid and High End Automotive: 1T Floating Gate Solutions</strong></td>
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<td></td>
</tr>
<tr>
<td>130nm Flash - Auto</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90nm Flash - Auto</td>
<td>FL</td>
<td>LC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65nm Flash - Auto</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- In Development
- In Production
- Customer Samples
- Process Qualification

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e200z Core Roadmap

Powertrain & Chassis

2004

2005

2006

2007

10-stage pipeline
Up to 32k cache
Dual Issue / VLE
FPU | SIMD
e200z7
264MHz

5-stage pipeline
Up to 16k cache
Dual Issue / VLE
FPU | SIMD
e200z4
120MHz

4-stage pipeline
VLE
FPU | SIMD
e200z3
80MHz

4-stage pipeline
VLE
FPU | SIMD
e200z1
80MHz

4-stage pipeline
VLE Only
e200z0
80MHz

7-stage pipeline
Up to 32k cache
VLE
FPU | SIMD
e200z6
200MHz

7-stage pipeline
Up to 32k cache
VLE
FPU | SIMD
e200z6
144MHz

4-stage pipeline
VLE
FPU | SIMD
e200z1
80MHz

Body Electronics

Performance / Features

This document contains forward-looking statements based on current expectations, forecast and assumptions of Freescale that involves risk and uncertainties. Forward looking statements are subject to risk and uncertainties associated with Freescale business that could cause actual results to vary materially from those stated or implied by such forward-looking statements.
### Powertrain Product Families Currently In Production

<table>
<thead>
<tr>
<th>Device</th>
<th>MPC5533</th>
<th>MPC5534</th>
<th>MPC5553</th>
<th>MPC5554</th>
<th>MPC5565</th>
<th>MPC5566</th>
<th>MPC5567</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Platform</td>
<td>Power e200z3</td>
<td>Power e200z3</td>
<td>Power e200z6</td>
<td>Power e200z6</td>
<td>Power e200z6</td>
<td>Power e200z6</td>
<td>Power e200z6</td>
</tr>
<tr>
<td>Program Flash</td>
<td>768 KB</td>
<td>1 MB</td>
<td>1.5 MB</td>
<td>2 MB</td>
<td>2 MB</td>
<td>3 MB</td>
<td>2 MB</td>
</tr>
<tr>
<td>SRAM</td>
<td>48 KB</td>
<td>64 KB</td>
<td>64 KB</td>
<td>64 KB</td>
<td>80 KB</td>
<td>128 KB</td>
<td>80 KB</td>
</tr>
<tr>
<td>DMA</td>
<td>32 Ch</td>
<td>32 Ch</td>
<td>32 Ch</td>
<td>64 Ch</td>
<td>32 Ch</td>
<td>64 Ch</td>
<td>32 Ch</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
<td>Emulated in program Flash</td>
</tr>
<tr>
<td>eSCI</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>DSPI</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>CAN</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Flexray</td>
<td></td>
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</tbody>
</table>
| Ethernet (100BaseT) | | | | | | | | ✓
| MLB | | | | | | | | 
| External Bus | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Nexus | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| ETPU | 32-Ch., | 32-Ch., | 32-Ch., | 2x32-Ch., | 32-Ch., | 2x32-Ch., | 32-Ch., |
| eMiOS | 24-Ch., 24-bit | 24-Ch., 24-bit | 24-Ch., 24-bit | 24-Ch., 24-bit | 24-Ch., 24-bit | 24-Ch., 24-bit | 24-Ch., 24-bit |
| GPIO | 192 | 192 | 220 | 256 | 192 | 256 | 238 |
| ADC | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit | 40-Ch., 1 x 12-bit |
| Voltage | 3.3V & 5V | 3.3V & 5V | 3.3V & 5V | 3.3V & 5V | 3.3V & 5V | 3.3V & 5V | 3.3V & 5V |
| Temp. Range | M | M | M | M | C, M | C, M | C, M |
| Frequency Range | 40-80MHz | 40-80MHz | 80-132MHz | 80-132MHz | 80-132MHz | 80-132MHz | 80-132MHz |
| Package Options | 208 MAPBGA, 324 PBGA | 208 MAPBGA, 324 PBGA | 208 MAPBGA, 324 PBGA, 416 PBGA | 416 PBGA | 324 PBGA | 416 PBGA | 324 PBGA, 416 PBGA |

**Note:** MPC5533 only has one ADC converter. All other MPC55xx devices have one 40 channel dual Enhanced queued analog-to-digital converter (eQADC) - each up to 12 bit resolution and up to 1.25us. The 208 pkg only supports 34 ADC channels.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5533 products in 208 MAPBGA packages; MPC5534 and MPC5553 products in 208 and 496 MAPBGA packages; MPC5554, MPC5565, MPC5566 and MPC5567 products in 496 MAPBGA packages.

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FSL Packaging Strategy: Maximize vertical and horizontal scalability

(1) the majority of I/O functions (eTPU, eMIOS, CAN, ADC) would use compatible locations, meaning that they occupy same general area of package ballmap, allowing minimized PCB redesign to transition
Nauru - MPC5631N: 640K Engine Controller with Data Flash

105 DMIPS from core, with embedded DSP and hw FPU; 1.6 DMIPS MHz at 64MHz; option of 80MHz version

12bit ADC with on-chip knock, built-in filtering system allows cost reduction of PCB

Most precise engine timers available, control fuel delivery & improve gas mileage, adds 32 DMIPS

Data flash (total 128K) allows cost effective EEPROM emulation
Mamba - MPC5674F: 4 MB Engine Controller with FlexRay™

600 DMIPS from 264 MHz core, integrated DSP allowing users to create ‘virtual sensors’

Only quadruple ADC on market, with built-in filtering system allows cost reduction of PCB

Most precise engine timers available, control fuel delivery & improve gas mileage

Largest program memory for market space helps with autocoding; zero defect technology on all memories

Power Technology
e200z7 superscalar CPU
SPE
MMU

4x Dec Fil
64 ch QUAD ADC

timed I/O system
eMOS 32ch.
eTPU 32ch.
eTPU data 32ch.

4MB Flash w/ ECC
256K SRAM w/ ECC (32K S/B)

600 DMIPS from 264 MHz core, integrated DSP allowing users to create ‘virtual sensors’

Only quadruple ADC on market, with built-in filtering system allows cost reduction of PCB

Most precise engine timers available, control fuel delivery & improve gas mileage

Largest program memory for market space helps with autocoding; zero defect technology on all memories

System integration
VReg
Osc/PLL
Interrupt Controller

2 x eDMA 64 & 32ch

4 MB Flash w/ECC
256K SRAM w/ECC (32K S/B)

Main memory system

EDB
development & calibration bus

Boot Assist Module (BAM)

Debug
JTAG
Nexus IEEE Isto 5001-2003

communications
4x FlexCAN
3x eSCI
4x DSPI
4x Dec Fil
64 ch QUAD ADCi
Core
- 80 MHz Power Architecture™ e200z3 Core + VLE
  - SPE Module for Floating Point & DSP
  - 8 Entry MMU

Memory
- Up To 1.5MB Byte RWW Flash with ECC
- Up To 111kB Total SRAM
  - Up To 94kB on chip static RAM (32kB standby) with ECC
  - 17kB for eTPU (14kB code & 3kB data)

I/O
- Timed I/O Channels
  - 32 channel eTPU2
  - 16 channel eMIOS
- 2 x FlexCAN - Compatible with TouCAN, 32/64 Message Buffers
- 2 x eSCI
- 2 x DSPI 16 bits wide up to 6 chip selects each
  - SPI with continuous mode and DMA support
  - Supporting Micro Second Bus, optionally using LVDS
- 34 channel Dual ADC - up to 12 bit and up to 670ns conversions
  - 6 Queues with triggering and DMA support
  - Variable Gain Amplifier (X1, X2, X4)
  - Decimation Filters
  - Temperature sensor and Absolute voltage reference

System
- FM-PLL
- 32 Channel enhanced DMA Controller
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STIM) (for AutoSAR task monitor function)
- Software Watchdog (SWaT) (windowing watchdog)
- Interrupt Controller (plus NMI)
- Nexus IEEE-ISTO 5001-2003 Class 2+ (ETPU Class 1)
- Single 5V Power supply is optional
- EBI for calibration (16/32bit)
- 100, 144 & 176 pins.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC563xM and MPC564xA products in 208 MAPBGA packages.
Andorra 4MB – MPC5644A

Core
- 145 MHz Power Architecture™ e200z4d Core + VLE
  - Dual Issue Core with SPE Module for Floating Point & DSP
  - 4kB Instruction Cache - 2 or 4 way - with error detection
  - 16 Entry MMU, NMI, Power Saving mode

Memory
- 4MB Byte RWW Flash with ECC
- 213kB Total SRAM
  - 192kB on chip static RAM (including 24kB standby) with ECC
  - 4kB unified-cache (with line locking)
  - 17kB for eTPU (14kB code & 3kB data)

I/O
- Timed I/O Channels
  - 32 channel eTPU2
  - 24 channel eMIOS
- FlexRay
  - Dual Channel (10MB/s)
- 3 x FlexCAN - Compatible with TouCAN, 64 Message Buffers Each
- 3 x eSCI
- 3 x DSPI 16 bits wide up to 6 chip selects each
  - SPI with continuous mode and DMA support
  - Supporting Micro Second Bus, optionally using LVDS
- 1 x CRC unit
- 40 channel Dual ADC - up to 12 bit and up to 670ns conversions
  - 6 Queues with triggering and DMA support
  - Variable Gain Amplifier (X1, X2, X4)
  - Dual Decimation Filters
  - Temperature sensor and Absolute voltage reference

System
- FM-PLL
- 64 Channel enhanced DMA Controller
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STIM) (for AutoSAR task monitor function)
- Software Watchdog (SWaT) (windowing watchdog)
- 378 source Interrupt Controller (plus NMI)
- Nexus IEEE-ISTO 5001-2003 Class 3+ (ETPU Class 1)
- Single 5V Power supply is optional for 208 and 176 QFP packages only
- EBI for calibration (16/32bit)
- 176 LQFP / 208MapBGA / 324PBGA (bus, 40ADC), KGD (no PGE Pads)

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Andorra 2M – MPC5642A Preliminary

**Core**
- 145 MHz Power Architecture™ e200z4d Core + VLE
  - Dual Issue Core with SPE Module for Floating Point & DSP
  - 4kB Instruction Cache - 2 or 4 way - with error detection
  - 16 Entry MMU, NMI, Power Saving mode

**Memory**
- 2MB Byte RWW Flash with ECC
- 149kB Total SRAM
  - 128kB on chip static RAM (including 32kB standby) with ECC
  - 4kB instruction cache (with line locking)
  - 17kB for eTPU (14kB code & 3kB data)

**I/O**
- Timed I/O Channels
  - 32 channel eTPU2 with 5 channel Reaction Module
  - 24 channel eMIOS
- FlexRay
  - 3 x FlexCAN - Compatible with TouCAN, 64 Message Buffers Each
  - 3 x eSCI
  - 3 x eSPI 16 bits wide up to 6 chip selects each
  - SPI with continuous mode and DMA support
  - Supporting Micro Second Bus, optionally using LVDS
- 1 x CRC unit
- 40 channel Dual ADC - up to 12 bit and up to 670ns conversions
  - 6 Queues with triggering and DMA support
  - Variable Gain Amplifier (X1, X2, X4)
  - Dual Decimation Filters
  - Temperature sensor and Absolute voltage reference

**System**
- FM-PLL
- 64 Channel enhanced DMA Controller
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STiM) (for AutoSAR task monitor function)
- Software Watchdog (SWaT) (windowing watchdog)
- 475 source Interrupt Controller (plus NMI)
- Nexus IEEE-ISTO 5001-2003 Class 3+ (ETPU Class 1)
- Single 5V Power supply is optional for 176 QFP packages only
- EBI for calibration (16bit)
- 176 LQFP / 324MapPBGA(bus, 40ADC), no KGD

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Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC563xM and MPC564xA products in 208 MAPBGA packages.
Cobra 6MB – MPC5776R Preliminary

Core
- 200 MHz Dual Power Architecture™ e200z7d Core + VLE
  - Dual Issue Core with SPE2 Module for Floating Point & DSP
  - 16kB Instruction & 16kB Data Cache
  - 16 Entry MMU & MPU

Memory
- 6MB Byte RWW Flash with ECC
- 461kB Total SRAM
  - 384kB on chip static RAM (48kB with standby) with ECC
  - 32kB unified-cache (with line locking)
  - 45kB for eTPU (36kB code & 9kB data)

I/O
- Timed I/O Channels
  - 3 x 32 channel eTPU2
  - 32 channel eMIOS
- FlexRay
  - Dual Channel (10MB/s)
  - 4 x FlexCAN - TouCAN Compatible, 64 Message Buffers Each
  - 3 x eSCI
  - 5 x DSPI 16 bits wide up to 6 chip selects each
  - SPI with continuous mode and DMA support
  - Supporting Micro Second Bus, optionally using LVDS
  - 1 x CRC unit
  - 4 x Protected Port Outputs
  - 64 channel Quad ADC - up to 12 bit & up to 670ns conversions
    - 12 Queues with triggering and DMA support
    - Variable Gain Amplifier (X1, X2, X4)
    - 10 Decimation Filter block with Hardware Knock Integrators
    - Temperature sensor and Absolute voltage reference

System
- FM-PLL
- Dual 64 Channel enhanced DMA Controller
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STiM) (for AutoSAR task monitor function)
- Software Watchdog (SWaT) (windowing watchdog)
- Dual Interrupt Controller (plus NMI)
- Nexus IEEE-ISTO 5001-2003 Class 3+ (ETPU Class 1)
- Single 5V Power supply is option
- EBI for calibration (16/32bit)
- 416 BGA KGD (no PGE Pads), proposed 516 BGA
Komodo 2MB – MPC5675K

**Core**
- 180+ MHz Dual Power Architecture™ e200z7d Core + VLE
  - Dual Issue Core with SPE2 Module for Floating Point & DSP
  - Lock Step Option with Redundancy Checking Hardware
  - 16K Instruction & 16K Data Cache for each core
  - 16 Entry MMU, NMI, Power Saving mode

**Memory**
- Up To 2MB Byte RW2 Flash with ECC
- Up To 512kB SRAM with ECC

**I/O**
- Timed I/O Channels
  - Motor Control Peripheral set for up to 3 motors
  - 3 x FlexPWM - with 8 channels each
  - 3 eTimer - with 6 channels each
  - 2 Cross Triggering Units for Autonomous Operation
  - 16 channel eMIOS
- Ethernet
- FlexRay
  - Dual Channel (10MB/s)
- 4 x FlexCAN - Compatible with TouCAN (1 Safety Port)
- 4 x LINFlex
- 3 x I2C
  - SPI with continuous mode and DMA support
- 1 x CRC unit
- PDI For CMOS Image Sensors
- 22 Channel Quad ADC - 1M Sample / Second
  - Temperature sensor and Absolute voltage reference

**System**
- FM-PLL
- Dual Interrupt Controllers with NMI
- 16 Channel enhanced DMA Controller
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STIM) (for AutoSAR task monitoring)
- Software Watchdog (SWaT) (windowing watchdog)
- Nexus IEEE-ISTO 5001-2003 Class 3+ (ETPU Class 1)
- EBI for Calibration & External Memory (DRAM Controller)
- 257BGA & 473BGA (Additional Packages TBD)

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Python Up To 6MB – MPC577x Concept

Core
- True Quad Core
- 200+ MHz Dual Power Architecture™ e200z7d Core + VLE
  - Dual Issue Core with SPE2 Module for Floating Point & DSP
  - 16K Instruction & 16K Data Cache for each core
  - 16 Entry MMU, NMI, Power Saving mode
- Dual e200 Zen Vector Cores with SPE for DSP Filtering

Memory
- Up To 6MB Byte RWW Flash with ECC
- Up To 512kB SRAM with ECC

I/O
- Timed I/O Channels
  - Motor Control Peripheral set for up to 2 motors
  - 3 x FlexPWM - with 8 channels each
  - 3 eTimer - with 8 channels each
  - Cross Triggering Unit for Autonomous Operation
  - 24 channel eMIOS
- FlexRay
  - Dual Channel (10MB/s)
  - 4 x FlexCAN - Compatible with TouCAN
  - 2 x eSCI
  - 4 x DSPI 16 bits wide up to 6 chip selects each
  - SPI with continuous mode and DMA support
  - Supporting Micro Second Bus, optionally using LVDS
  - 1 x CRC unit
  - 64 channel Quad ADC - 1M Sample / Second
    - Temperature sensor and Absolute voltage reference

System
- FM-PLL
- Dual Interrupt Controllers with NMI
- Dual 64 Channel enhanced DMA Controllers
- Peripheral Interrupt Timer (PIT) (capable of queue triggering)
- System Timer Module (STIM) (for AutoSAR task monitoring)
- Software Watchdog (SWaT) (windowing watchdog)
- Nexus IEEE-ISTO 5001-2003 Class 3+ (ETPU Class 1)
- EBI for calibration (16/32bit)
The Crossbar Architecture, a Turbo for Gateways

- Platform = cores + crossbar + system support functions (INTC, debug, timers, semaphores...)

- The crossbar switch allows concurrent accesses between masters and slaves resources

- Widening the memory bottleneck:
  - Separate SRAM blocks
  - Flash controller with separate page buffers to emulate dual-ported flash

- Peak data bandwidth of the MPC5668G crossbar architecture is 3.5 Gbytes/sec at 116 MHz clock speed
Agenda

► Freescale Overview, Vision, Trends and Quality
► Why Freescale for Powertrain?
► Powertrain Performance
► Technology Roadmap
► Powertrain Overview & Roadmaps
► Addressing Powertrain Customer Challenges
► Summary and Q&A
Direct Injection Improves Fuel Efficiency by 15-20%

- Direct injection used for both gasoline and “clean” diesel systems to boost fuel economy

- Engine gear teeth can be measured every 6 degrees
  - 1/10th degree accuracy is needed for optimal control of fuel spray and spark

**MCU input data is less accurate than the required output, therefore the MCU has to ‘predict’ when to spark**

- Uses eTPU to predict and compensate for precise engine control and mechanical limitation
  - Measures time between the last 2 teeth and makes angle to time conversions
  - Needs significant performance to do ~36,000 conversions/sec per cylinder
  - Improves fuel economy through tighter control yields
Knock Detection Using Power Architecture

► Knock control systems
- Improves fuel economy by up to 3-5% by optimizing combustion cycle
- Requires more components, typically a dedicated knock chip
- Finds the knock signal from within engine noise (1/1000 of a second time window)
- Digitizes the signal and feeds back via the spark control system, typically 150 KHz

► Power Architecture handles this complexity
- Enhanced time processor unit (eTPU2) predicts the knock window
- Analog knock signal has to be digitized
- ADC is capable of reading 800 KHz, so it can comfortably sample knock and still have time to read other analog inputs in the system
- Decimation filters included to support the most advanced systems

► System cost savings
- Eliminates need for knock chip, filters, external ADC and multiplexer

All MPC56xx devices will support Knock implementation
Diesel Timing

Customer Challenges

► Accurate timing control is critical for emissions, fuel economy, performance, and noise.
  • Require precise multiple input of the high pressure fuel for each combustion event
► Very tight emissions regulations require precise sensing systems
► Need control of fuel pump and high voltage boost for direct injection

Freescale Solutions

► High accuracy, high resolution, tightly coupled timer systems (eTPU and eMIOS)
  • Complex input/output timer functions of the MPC5500 family are performed by enhanced time processor unit (eTPU) engines
    ▪ Each eTPU engine controls hardware channels, providing a total of 64 (24-bit) hardware, double action channels. Variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions.
  • Less complex timer functions of the MPC5500 family are performed by the enhanced modular input/output system (eMIOS).
    ▪ 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations.
► High performance CPU (portfolio includes products up to 300MHz)
► Future C90 devices offer close loop current control in H/W with integrated multiple current thresholds and edge timers

More examples
Agenda

► Freescale Overview, Vision, Trends and Quality
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► Summary and Q&A
Summary

► Recognized leader and exceptional quality record within Automotive Powertrain

► Partnering with our customers to address current and future automotive challenges (Cost, Schedule, Regulatory, etc…)

► Scalable and differentiated product line serving the ultra low-end to the high-end Powertrain markets

► Most powerful Powertrain architecture (PowerArchitecture)

► Robust Enablement environment