Migrating from the MPC8360E to the MPC8569E PowerQUICC® Processor

Overview of the hardware and software differences and concerns (Version 1)

Johnson Leung
Application Engineering
### Customer's Equipment I/O Requirements

<table>
<thead>
<tr>
<th>I/O: up to 16 TDMs, 4 GbE or 8 FE, one Utopia / POS Multi-PHY Level 2 (16 bit), one x4 PCI Express® (PCIe), one 4x Serial RapidIO® (sRIO) or Dual 1x sRIO</th>
<th>MPC8569E</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.33 GHz e500 CPU core, 512 KB L2 cache</td>
<td>Datapath offload in QUICC Engine™ module (4 RISC)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O: up to 8 TDMs, 5 GbE or 8 FE, two Utopia / POS Level 2 (16 bit), one x8 PCIe, one x4 sRIO</th>
<th>MPC8568E</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.33 GHz e500 CPU core, 512 KB L2 cache</td>
<td>Datapath offload in QUICC Engine module (2 RISC)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O: up to 8 TDMs, 2 GbE or 8 FE, two Utopia / POS Multi-PHY Level 2 (16 bit), one PCI</th>
<th>MPC8360E</th>
</tr>
</thead>
<tbody>
<tr>
<td>667 MHz e300 CPU core, no L2 cache</td>
<td>Datapath offload in QUICC Engine module (2 RISC)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O: up to 2 TDMs, 3 FE, one Utopia Multi-PHY Level 2 (8 bit), one PCI</th>
<th>MPC8323E</th>
</tr>
</thead>
<tbody>
<tr>
<td>333 MHz e300 CPU core, no L2 cache</td>
<td>Datapath offload in QUICC Engine module (1 RISC)</td>
</tr>
</tbody>
</table>
Migration to E500, DDR3, PEX, SRIO and more...
MPC8569E PowerQUICC III: Bridging the Gap to the All-IP Network

- **e500v2 core**, built on Power Architecture® Technology, from 800 MHz to 1.33 GHz
  - 512 KB L2 Cache w/ ECC
  - 36-bit physical addressing
  - Double precision floating point

- **System Interfaces**
  - 64b or 2x32-bit DDR2/3 w/ ECC
  - 800 Mbps/pin data rate
  - 16-bit Local Bus for SRAM/flash
  - Timers, DUART, 2xI²C, GPIO, SPI
  - USB 2.0 full speed

- **4 Lanes High Speed Serial Interfaces**
  - Dual SGMII
  - Dual 1x (or one 4x) Serial RapidIO®
  - x1, x2, x4 PCI Express®

- **QUICC Engine**
  - 4 RISCs up to 667 MHz
  - Maximum of 8 Ethernet interfaces, one per UCC:
    - 4 x Gigabit Eth (up to 2 w/SGMII)
    - Up to 8 x 10/100 Ethernet
  - Multi-PHY UTOPIA/POS-PHY L2 (16-bit)
  - IEEE® 1588 Support v2
  - 16 x T1/E1 (512 x 64kbps channels)

- **Security Engine (SEC 3.1)**
  - ARC4, 3DES, AES, RSA/ECC, RNG, XOR, Single pass SSL/TLS, Kasumi, SNOW

- **Four-channel DMA**
- **45 nm SOI process technology**
- **Target <7W Power (@ 800 MHz e500)**
E500v2, DDR3 and more…

► E500v2
  • 2799 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  • 36-bit physical addressing, up to 64G-bytes addressing space
  • Double-precision (64-bits) floating-point APU and Embedded vector and scalar
    single-precision floating-point APUs
  • 512 Kbytes of L2 cache/SRAM

► DDR3 Support
  • SSTL-1.8, and SSTL-1.5 compatible IOs
  • New DDR3 initialization sequence supported
  • DDR3 ZQ Calibration Command and Write Leveling control
  • Supports address parity for registered DIMMS
  • Supports DDR3 Burst Chop on the fly by A12 for 8-byte burst

► Other Enhancements
  • eLBC NAND Flash support
  • eSDHC support for SD/MMC card interface
  • SEC3.1: Protocol support includes ARC4, 3DES, AES, RSA/ECC, RNG, Single-pass SSL/TLS, Kasumi, SNOW, XOR acceleration
4 Lanes Flexible High-Speed Interconnect Interfaces

- Dual SGMII
- Dual 1x (or one 4x) Serial RapidIO®
- x1, x2, x4 PCI Express®

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Lanes</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>e</td>
<td>b</td>
</tr>
<tr>
<td>1</td>
<td>SGMII</td>
<td>SGMII</td>
</tr>
<tr>
<td>2</td>
<td>SGMII</td>
<td>SGMII</td>
</tr>
<tr>
<td>3</td>
<td>SGMII</td>
<td>SGMII</td>
</tr>
<tr>
<td>4</td>
<td>1xSRIO</td>
<td>1xSRIO</td>
</tr>
<tr>
<td>5</td>
<td>1xSRIO</td>
<td>1xSRIO</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>1xSRIO</td>
</tr>
<tr>
<td>10</td>
<td>SGMII</td>
<td>SGMII</td>
</tr>
</tbody>
</table>
Migration to New QUICC Engine
## Device Migration

<table>
<thead>
<tr>
<th>Product Family</th>
<th>MPC8560E</th>
<th>MPC8360E</th>
<th>MPC8568E</th>
<th>MPC8569E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Control</td>
<td>e500</td>
<td>e300</td>
<td>e500</td>
<td>e500</td>
</tr>
<tr>
<td>Max Core Frequency</td>
<td>1 GHz</td>
<td>667 GHz</td>
<td>1.33/1.5GHz</td>
<td>1.33 GHz</td>
</tr>
<tr>
<td>CPM or QE</td>
<td>CPM</td>
<td>QE</td>
<td>QE</td>
<td>QE</td>
</tr>
<tr>
<td>No of RISC</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>CPM/QE Memory</td>
<td>32K IRAM, 32K MURAM</td>
<td>48K IRAM, 48K MURAM, 192K ROM</td>
<td>64K IRAM, 64K MURAM, 192K ROM</td>
<td>256K IRAM, 128K MURAM</td>
</tr>
<tr>
<td>Max CPM/QE Frequency</td>
<td>333 MHz</td>
<td>Up to 500 MHz</td>
<td>Up to 533 MHz</td>
<td>Up to 667 MHz</td>
</tr>
<tr>
<td>Ethernet (MII, RMII)</td>
<td>3</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Ethernet (GMII, RGMII)</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>4 (include 2 SGMII)</td>
</tr>
<tr>
<td>ATM UTOPIA M-PHY</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>POS-PHY</td>
<td>-</td>
<td>2x128</td>
<td>1x31</td>
<td>1x128</td>
</tr>
<tr>
<td>TDMs</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>MCC (256 HDLC ch)</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>USB (full/low speed)</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>SPI</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Encryption (Option)</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>IEEE 1588</td>
<td>-</td>
<td>Y (V2)</td>
<td>-</td>
<td>Y (V2)</td>
</tr>
<tr>
<td>Availability</td>
<td>Now</td>
<td>Now</td>
<td>Now</td>
<td>Sampling</td>
</tr>
<tr>
<td>Process</td>
<td>130 nm</td>
<td>130 nm</td>
<td>90 nm SOI</td>
<td>45 nm</td>
</tr>
<tr>
<td>Package</td>
<td>783 FC-PBGA</td>
<td>668 PBGA</td>
<td>740 TBJA</td>
<td>1023 FCPBGA</td>
</tr>
<tr>
<td>Typical Power</td>
<td>16.5W @ 1GHz</td>
<td>3-3.5W PBGA, 5-7W TBGA</td>
<td>13-19W Est</td>
<td>&lt;7W@800 MHz core (&lt;10W@1.33 GHz core)</td>
</tr>
</tbody>
</table>
QUICC™ Engine – Architecture: Flexible, Scalable and Packet-friendly

- Asynchronous architecture scaling from one to four RISCs at 200-667 MHz
  - Code compatible
  - Compatible with existing PowerQUICC® CPM architecture
- Eight unified communication controllers (UCCs) support virtually any interface
  - 10/100/1000 Gigabit Ethernet
  - Utopia / POS Multi-PHY Level 2 ports
  - Serial ATM
- Multi-channel communications controller supporting time multiplexed protocols
  - Supports up to 16 T1/E1 interfaces
  - 256 HDLC or 128 SS7 channels on 8 TDMs
  - Serial ATM (up to 64 TC layers)
  - ML/IC/PPP
- Support for SPI, USB and other interfaces
- Protocol termination and interworking for a wide range of communication protocols including ATM, Ethernet, PPP, HDLC, TDM, UTOPIA and POS

<table>
<thead>
<tr>
<th></th>
<th>MPC832x</th>
<th>MPC8360</th>
<th>MPC8569</th>
</tr>
</thead>
<tbody>
<tr>
<td>No of RISCs</td>
<td>1 RISC</td>
<td>2 RISC</td>
<td>4 RISC</td>
</tr>
<tr>
<td>MHz Range</td>
<td>200</td>
<td>200-533</td>
<td>200-667</td>
</tr>
<tr>
<td>IRAM Memory</td>
<td>8K Bytes</td>
<td>48K-64K Bytes</td>
<td>256K Bytes</td>
</tr>
<tr>
<td>MURAM Memory</td>
<td>16K Bytes</td>
<td>48K-64K Bytes</td>
<td>128K Bytes</td>
</tr>
<tr>
<td>ROM Memory</td>
<td>96K Bytes</td>
<td>192K bytes</td>
<td>N/A</td>
</tr>
<tr>
<td>Ethernet Ports</td>
<td>Up to 3 x 10/100</td>
<td>Up to 8 x 10/100</td>
<td>Up to 8 x 10/100</td>
</tr>
<tr>
<td></td>
<td>(up to 3 x 10/1000)</td>
<td>(up to 4 x 10/1000)</td>
<td></td>
</tr>
<tr>
<td>UTOPIA/POS Ports</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>TDM ports</td>
<td>4</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>IEEE1588 Support</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Comprehensive CodeWarrior™ and 3rd-Party Enablement Ecosystem
RISC Complex and Task Scheduling Enhancement

► 4 x RISC Complex (compared to 2 x RISC in MPC8360)
  • More RISCs means: increased performance and a decrease in overall QE bandwidth consumed depending on type of traffic.
  • The micro code is architected such that it is agnostic to the number of RISCs so it is not designed for a particular QE version.
  • Number of RISCs is transparent to the user, one set of interface registers (QE command, command data, etc.)

► Enhanced match accelerator suitable for large key comparison
  • Enhance performance in IPv6 application where larger keys are needed

► Supports up to 128 tasks (80 tasks in MPC8360)
  • 48 additional Internal Virtual Threads (QE internal triggered)
  • Support QE external triggered External Virtual Threads (SRIO, SEC)
Internal Memories and SDMA Enhancement

► Multi User RAM
  • 128 KByte (48KByte on MPC8360)
  • 8 bank interleaved (4 bank interleaved on MPC8360)
► Instruction RAM
  • 256KByte (48Kbyte on 8360), No ROM (192KByte on 8360)
  • Big enough to fit all of the micro code for a full application
  • 8 bank interleaved (4 bank interleaved on 8360)
  • Microcode image is shared between the RISCs
► SDMA (Serial DMA)
  • SDMA queue of 30 Entries + 1 Entry for high priority (12+1 in MPC8360),
    for each bus (system bus and local bus)
I/O Interface Enhancement

► TDM
  • Up to 16 T1/E1/J1/E3 or DS-3 serial interfaces
    ▪ Two MCCs, 256 channel each (Only one MCC in MPC8360)
    ▪ Two SI TDMs, support 8 TDMs and hooks to its own MCC (Only one SI in MPC8360)

► Ethernet
  • Up to eight 10/100-Mbps Ethernet interfaces using RMII
  • Up to four 1000-Mbps Ethernet interfaces using
    ▪ Four RGMII/RTBI, or
    ▪ Two RGMII/RTBI and two SGMII, or
    ▪ Two RGMII/RTBI and one GMII, or
    ▪ Two GMII and two SGMII
Migration on Software
Protocol Suite and Interfaces

- **Virtual Port**
  - IP FWD
  - Parsing Look-Up
  - IP fragmentation
  - IP Reassembly
  - IP Header compression/Decompression

- **IPsec**
  - Virtual Port

- **AAL-2**
  - I.366.2
  - AAL-2 Switching

- **AAL-0**

- **AAL-1**

- **AAL-2**
  - I.366.1

- **AAL-5**

- **ATM Low Layer Module**

- **Utopia Interface 128 PHYs**

- **IPoA & PPPoA**
  - RFC 2516

- **PPP MUX**
  - RFC 3153

- **PPP**
  - RFC 1661
  - RFC 1662

- **HDLC/Transp**

- **TDM**

- **TC - SAM**

- **IMA**

- **SS7/ESS7**

- **Circuit Emulation Services (CES)**

- **QMC**

- **Cell Switch**

- **MSP**

- **PPP ML/MLC**
  - RFC 1990/2686

- **POS**

- **PPP MUX**

- **Eth to ATM Bridging**

- **VLAN&QoS**
  - RFC 2684

- **PPPoE**
  - RFC 2516

- **PPP MUX**
  - RFC 3153

- **PPP**
  - RFC 1661
  - RFC 1662

- **L2 SW**
  - 802.3 MAC

- **L2 SW**

- **TPoA & PPPoA**
  - RFC 2516

- **IPsec**
  - Alpha release Oct, 09

- **Partial IP Reassembly: Now Full IP Reassembly: Dec, 09**

- **IP fragmentation**

- **IP Header compression/Decompression**

- **IP FWD**

- **Parsing Look-Up**

- **ATM Policing**

- **ATM Layer Module**
<table>
<thead>
<tr>
<th>MPC8360 Packages Release</th>
<th>AE_B_2.3.0</th>
<th>PE_A_2.3.1</th>
<th>PE_B_2.3.1</th>
<th>PAE_C_1.1.0</th>
<th>EE_D_0.0.2</th>
<th>PS_T_0.0.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet Termination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ethernet Hierarchical Scheduler</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ATM Termination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ML/MC PPP Termination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PPPMux</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESS7 Termination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POS Termination</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2E IW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2E IW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2E IW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HC/Hdec IW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HC/Hdec IW IP only</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP Reassembly</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP Fragmentation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtual Port IW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Longest Prefix Match</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

► 8569 has 256K-Bytes IRAM (no IROM). At this time there is only one image of the code
QUICC Engine™ Netcomm Device Drivers Overview

► Device Drivers:
  • Modular set of platform, peripheral and protocol device drivers
  • Operating system independent APIs (e.g. bare board) for customer application use and porting
    - Operating system porting guide provided
  • Platform level drivers supported – MMU, cache, interrupt controller, memory controllers, timers, DUART, I²C, security, etc.
  • Built-in use cases demonstrating functionality and performance
  • Complete device driver source code and comprehensive documentation provided

► Comprehensive feature set, including:
  • Interrupt or polling modes for communication peripherals
  • Statistics gathering
  • Protocol interworking
  • Support for both default (simple) and advanced (detailed) driver configurations
  • External memory management for parameters, tables and BD’s
  • Memory management support for system bus, secondary bus and local bus

► Hardware support:
  • Support for MDS processor and I/O boards
Previous Architecture (Release 2.3)

Use Case

- Low Level Driver
- Hardware

Low Level Driver

Hardware

HDL

Hardware Dependent Layer
New Architecture

Use Case

HAL
Hardware Abstraction Layer

HDL
Hardware Dependent Layer

Low Level Driver

Low Level Driver

Hardware

Hardware
New Architecture

Use Case

Device Manager Interface

HAL
Hardware Abstraction Layer

HDL
Hardware Dependent Layer

Wrapper

Low Level Driver

Hardware

Wrapper

Low Level Driver

Hardware
QUICC Engine™ Linux® Drivers

QUICC Engine Linux driver package contains:
► Low-level drivers
► (bare board)
► User space libraries

► The user space API is a mirror of the bare board API

Supported features include:
► Ethernet termination
► ATM termination
► IMA termination
► PPP termination
► ATM2ETH interworking
► ETH2ETH interworking
► PPP2ETH interworking
► ATMoIMA2ETH interworking
► Packet filtering
MPC8569E: Optimizing Power and Cost

- Integrated network control and data-plane in one device
- “All-IP” and multi-protocol networking under one hood
- 2.4x QUICC Engine performance enhancement
- IRAM and MURAM increase, no headache on microcode package
- Autonomous interworking support offloads e500 core
- Addressing future packet timing and security challenges