

1 Introduction

1.1 Purpose

This application note introduces the i.MX 8M Mini architecture by highlighting the differences from the i.MX 8M series processor upon which it is based. This document is a migration guide for developers that migrate from the i.MX 8M to the i.MX 8M Mini processor.

1.2 Scope

The i.MX 8M Mini architecture introduces new features which are different from the i.MX 8M. The i.MX 8M Mini also removes some features from i.MX 8M. The key differences include:

- Reduced the package size from 17×17 mm, 0.65 mm pitch to 14×14 mm, 0.5 mm pitch.
- Optimized power consumption.
- Increased Arm® Cortex®-A53 core platform frequency.
- Increased Arm® Cortex®-M4 target frequency.
- Removed display controller subsystem (DCSS), so HDR and Dolby vision is not supported.
- GPU 3D changed from GC7000 lite to GCNanoUltra, Single Shader support, OpenCL/Open Vision/Vulkan is not natively supported.
- Added 2D engine GC320, can use 2D for Color Space Conversion (CSC) and buffer transfers.
- Added one video encoder, the decoder performance is 1080p60.
- Added PDM audio input support.
- Supported 192 kHz audio on SPDIF interface.
- Increased lanes on SAI-2/3 from 1TX+1RX to 2TX+2RX lanes, with support for 768 kHz audio.
- Changed 2×USB3.0 to 2 ×USB2.0.
- Removed second PCIE and second MIPI CSI, do not affect the software.
- Removed HDMI interface.
- Added third SD/eMMC interface.
- Added third SDMA for audio interface.

Due to a close alignment to the i.MX 8M design, this document is structured as a summary of changes to the i.MX 8M Mini features. It provides references to modules that are reused or modified on the i.MX 8M Mini.

Contents

1 Introduction	1
1.1 Purpose.....	1
1.2 Scope.....	1
1.3 Audience.....	2
2 Feature Change Summary	2
2.1 BSP support.....	2
2.2 Module change list.....	2
2.3 Power.....	4
3 Revision history	5



1.3 Audience

This document is intended for system integrators and software developers migrating from the platforms based on the i.MX 8M.

2 Feature Change Summary

2.1 BSP support

The i.MX 8M Mini is supported by Linux BSP starting from [Linux_4.9.123-2.3.0_GA](#) release.

2.2 Module change list

This section summarizes the architectural changes of the i.MX 8M with respect to the i.MX 8M Mini. Table 1 compares the features of i.MX 8M Mini and i.MX 8M.

Table 1. Architectural changes

Category	Feature	Change from i.MX 8M	Board impact	Software impact
Assembly	Package size and pins	Updated	<ul style="list-style-type: none"> • Optimized for size and system cost <ul style="list-style-type: none"> — 14 × 14 mm package — 0.5 mm BGA pin pitch — 485 pins — Package design to use low cost drilled vias — 3.2 mil trace and space escape — Optimized power placements • Accommodated decouple caps under the BGA <ul style="list-style-type: none"> — Optimized for LPDDR4 routing — 6 to 8 layers fanout depending on signals and power usages 	None
Power	Power consumption	Optimized	Reduced the board level power further.	None

Table continues on the next page...

Table 1. Architectural changes (continued)

ARM® Cortex®-A53 core platform	Cortex-A53 core	Updated	Refer to Hardware Developer's Guide (HDG) to size Arm power supply appropriately.	Increased ARM® Cortex®-A53 core platform frequency from 1.4 GHz to 1.8 GHz. Modified the L2 cache from 1 MB to 512 KB.
Arm® Cortex®-M4 core platform	Cortex-M4 core	Updated	None	Increased the Arm® Cortex®-M4 target frequency from 266 MHz to 400 MHz.
GPU	GPU 3D	Updated	Changed GPU 3D from GC7000Lite to GCNanoUltra.	Reduced Open GL ES from 3.1 to 2.0. Added Open VG 1.1 support. Single Shader support, OpenCL/ Open Vision/ Vulkan not natively supported.
	GPU 2D	New	Added GPU 2D engine GC320.	The GC320 support code is added.
Display controller	DCSS	Removed	None	The DCSS support code is removed.
	HDR10, Dolby Vision	Removed	None	None
Video	Video Decoder	Updated	Reduced decoder performance from 4Kp60 to 1080p60.	None
	Video Encoder	New	Added 1080p60 H.264 1080p60 VP8 video encoder.	The video encoder support code is added.
Audio	PDM input	New	Added PDM audio input.	The PDMsupport code is added.
	SAI	Updated	Increased number of lanes on SAI-2/3 from 1TX+1RX to 2TX +2RX lanes, with support for 768 kHz audio.	None
	S/PDIF	Updated	Removed the second S/PDIF interface. Support 192 kHz audio on S/PDIF interface.	None
DMA	SDMA	Updated	Added third SDMA for audio interface.	The 3rdSDMAconfig code is added.
Connectivity	HDMI 2.0a	Removed	None	None
	MIPI-CSI	Removed	Removed the second MIDI-CSI interface.	None
	PCIe	Removed	Removed the second PCIe interface.	None
	USB	Updated	Changed 2 × USB3.0 to 2 × USB2.0.	None
External memory	SD/eMMC	Updated	Added third SD/eMMC interface.	The 3rdSD/eMMCconfig code is added.

Table continues on the next page...

Table 1. Architectural changes (continued)

On-chip memory	Boot ROM	Updated	Increased ROM size from 128 KB to 256 KB.	None
	OCRAM	Updated	Increased OCRAM size from 128 KB to 256 KB.	None
Security	High Assurance Boot (HAB)	Updated	None	HAB version is updated to 4.3.9.
System Integration	Memory Map	Updated	Memory map was updated to reflect IP changes.	Refer to Memory map chapter in the Reference Manual for full details.
	IRQ Map	Updated	IRQ map was updated to reflect IP changes.	Refer to IRQ map chapter in the Reference Manual for full details.
	DMA Map	Updated	DMA map was updated to reflect IP changes.	Refer to DMA map chapter in the Reference Manual for full details.
	Fuse Map	Updated	Fuse map was updated to reflect IP changes.	Refer to Fuse map chapter in the Reference Manual for full details.

2.3 Power

Figure 1. on page 5 shows the power trees of both i.MX 8M Mini and i.MX 8M. For i.MX 8M Mini, VDD_GPU supply is combined with VDD_VPU, VDD_DRAM and VDD_DRAM_PLL_0P8 on the EVK board, and VDD_SOC is combined with VDD_ARM_PLL_0P8, VDD_ANA_0P8, VDD_USB_0P8 and VDD_PCI_0P8 on the EVK board.

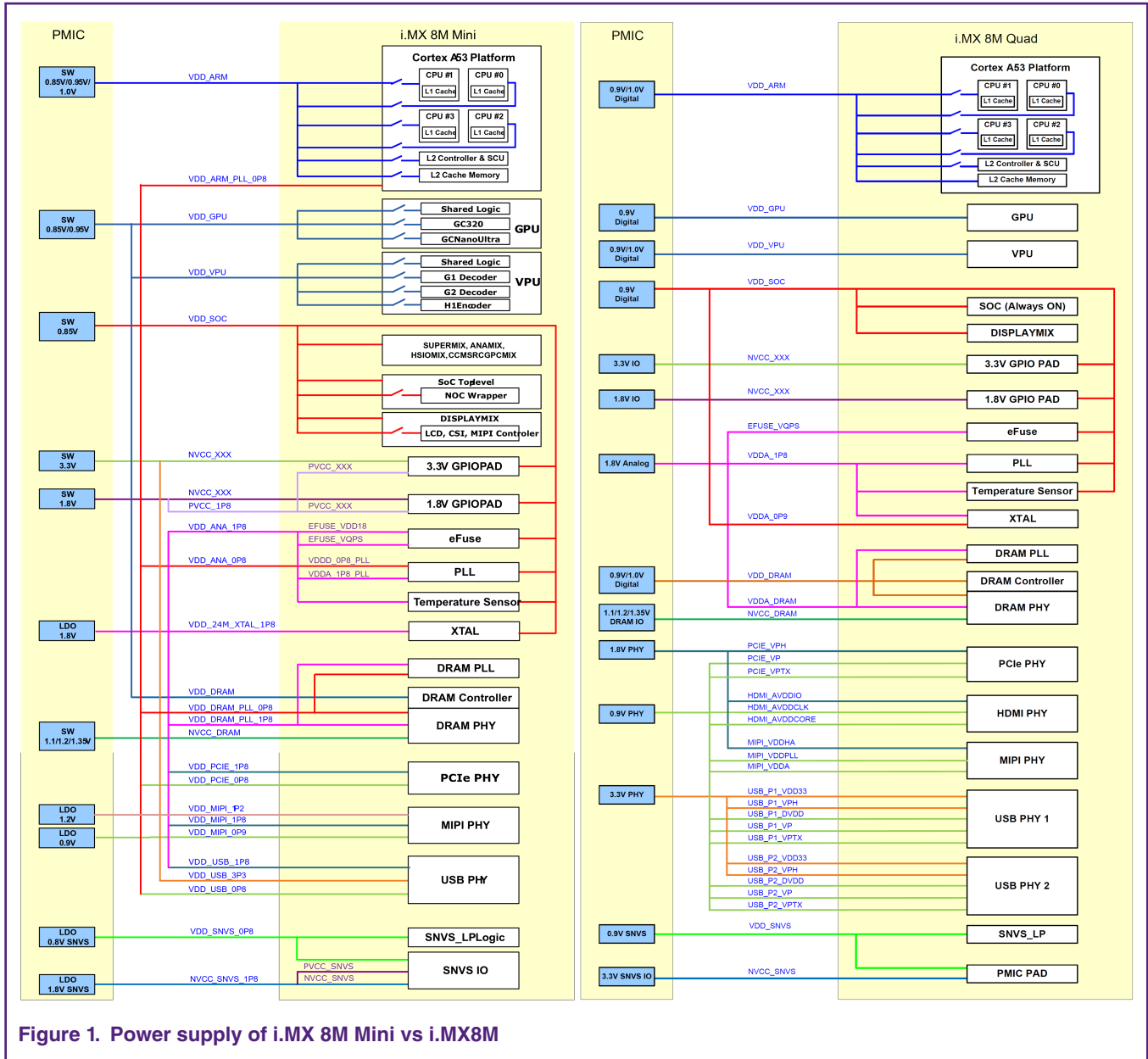


Figure 1. Power supply of i.MX 8M Mini vs i.MX8M

3 Revision history

Table 2. Revision history

Revision number	Date	Substantive changes
0	04/2019	Initial release

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 April 2019

Document identifier: AN12296

