NXP Semiconductors
Application Note

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Implementing the MC33903/4/5 CAN and LIN system basis chip

1 Introduction

This document provides in-depth guidance for module design and development implementing the MC33903/4/5 CAN-LIN System Basis Chip (SBC). This guidance will assist hardware and software engineers to develop safe, reliable, and robust automotive application modules. A detailed description of the SMARTMOS device operation features and their application usage is provided to ease the module's design and development. This specific application note covers the following topics:

- Device Segmentation
- Supply Voltage
- Embedded Regulators
- Multiplexer
- Serial Peripheral Interface (SPI)
- Configurable I/Os
- $\overline{\text{SAFE}}$, $\overline{\text{RST}}$, and $\overline{\text{INT}}$ Safe modes
- CAN and LIN Physical Layers
- Hardware Design
- Crank Pulse Handling
- Extending Current Capability on Vaux
- Programming the SBC
- Debug Mode
- SBC Initialization
- Enhanced Diagnostics
- Advanced Watchdog
- Low Power Modes
- Secured SPI
- Normal Request, Reset, and Flash Modes

Contents

1 Introduction 1
2 General information. 2
3 Device features 10
4 Hardware design 17
5 Programming the SBC 40
6 References 87
7 Revision history. 88

2 General information

2.1 MC33903/4/5 at a glance

The MC33903/4/5 System Basis Chip (SBC) is NXP Semiconductors' latest generation of SBCs designed and developed for automotive body multiplexing applications requiring CAN and LIN communication. These products offer enhanced diagnostics for functional safety and optimized multiple low power modes for low module current consumption.

The MC33903/4/5 SBC features NXP's robust CAN and LIN physical layers, which have been approved by multiple automotive Original Equipment Manufacturers (OEMs). These devices also have multiple 5.0 V or 3.3 V embedded regulators, robust I/Os, high accuracy voltage monitoring, multiplexer, fail-safe output, and enhanced SPI communication.

2.2 SBC device family concept

2.2.1 Device variations

The MC33903/4/5 SBC device family is composed of fourteen different products, which combine one or more transceivers, Low Drop Out (LDO) voltage regulators, I/Os, voltage monitoring, MUX output, and other features as shown on **Table 1**, **Table 2**, and **Table 3**:

Table 1. 33905 device variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
33905 (Dual LIN)	3.3 V or 5.0 V	2	2 Wake-up + 2 LIN terms or 3 Wake-up + 1 LIN terms or 4 Wake-up + no LIN terms	SOIC 54 pin exposed pad	Yes	Yes	Yes
33905S (Single LIN)		1	3 Wake-up + 1 LIN terms or 4 Wake-up + no LIN terms				

Table 2. 33904 device variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
33904	3.3 V or 5.0 V	0	4 Wake-up	SOIC 32 pin exposed pad	Yes	Yes	Yes

Table 3. 33903 device variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
33903	3.3 V [(1)] or 5.0 V [(1)]	0	1 Wake-up	SOIC 32 pin exposed pad	No	No	No
33903D (Dual LIN)	3.3 V or 5.0 V	2	1 Wake-up + 2 LIN terms or 2 Wake-up + 1 LIN terms or 3 Wake-up + no LIN terms			Yes	Yes
33903S (Single LIN)		1	2 Wake-up + 1 LIN terms or 3 Wake-up + no LIN terms				
33903P		0	3 Wake-up				

Notes
1. V_{DD} does not allow usage of an external PNP on the 33903. Output current limited to 100 mA.

2.2.2 Pin compatibility

The feature set of ALL the SBCs described in this document is 100% compatible amongst all device part numbers. The SBC family is divided in two separate groups of devices that implement pin compatibility. The pin compatibility of each of the groups eases the transition of going from one part number to another and prevents having to re-layout a module in case of last minute module functionality requirement changes. One of the pin compatible groups is made up of the MC33905D, MC33905S, MC33904, and MC33903 as shown in Figure 1

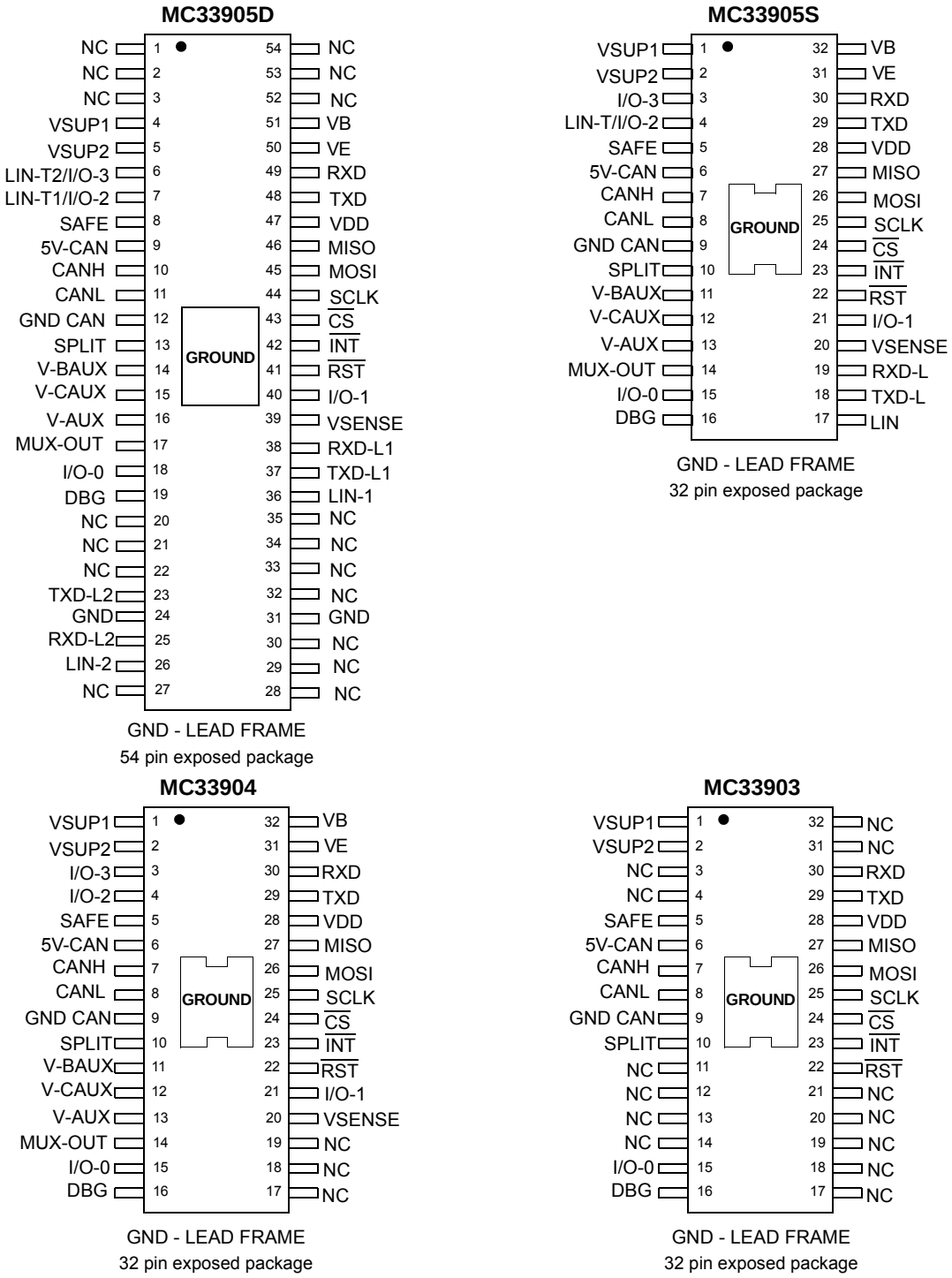


Figure 1. MC33905D, MC33905S, MC33904, and MC33903 pin connections

Something to note about this pin compatible group is that although the MC33905D is a 54 pin SOIC package, its footprint is still pin compatible to the rest of the 32 pin SOIC devices. Pin compatibility is accomplished by offsetting the placement of the smaller package by 3 pins down on the 54 pin footprint as shown in Figure 2

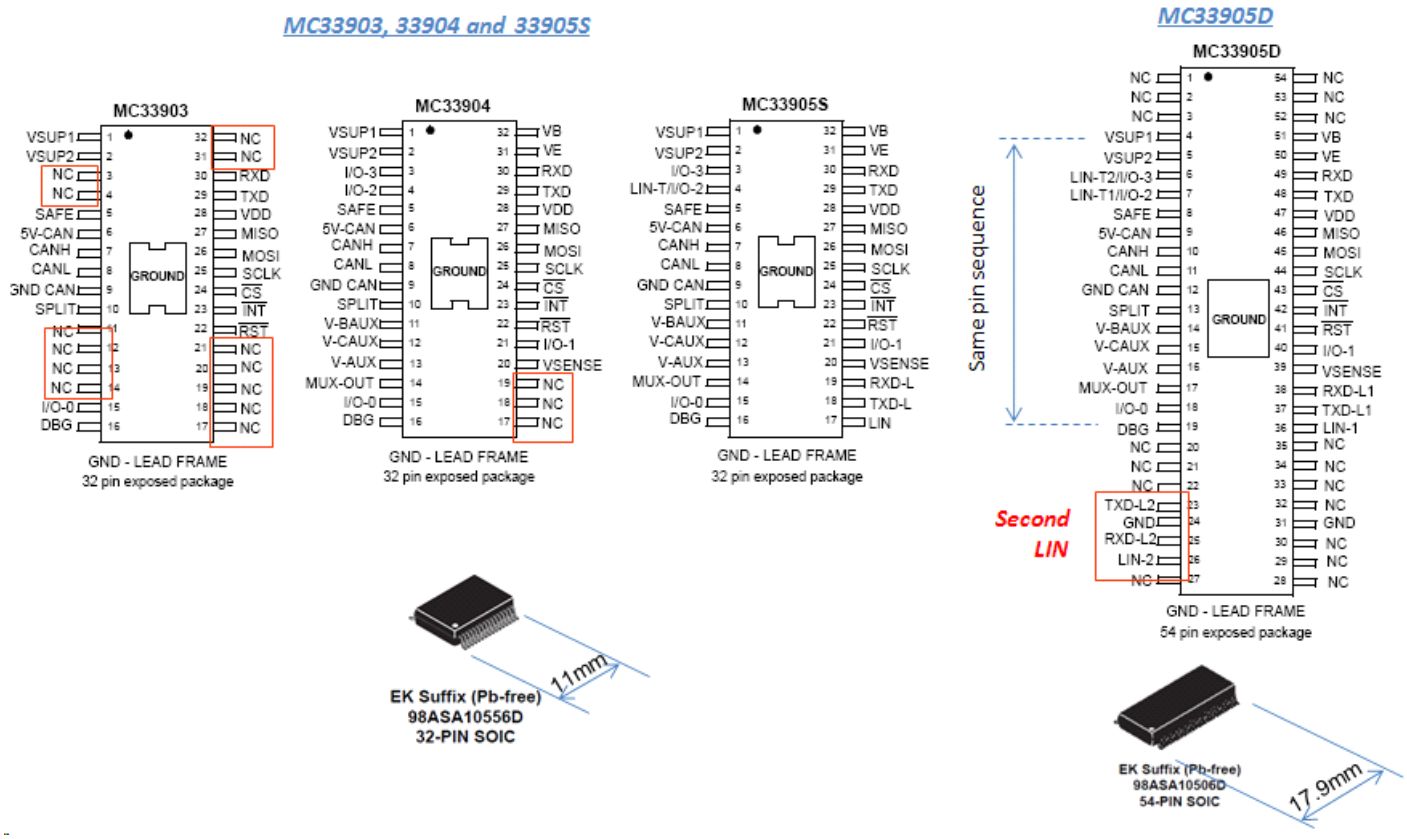


Figure 2. MC33905D, MC33905S, MC33904, and MC33903 pin compatibility

One other item to consider when laying out the Printed Circuit Board (PCB) is the implementation of the exposed pad to maximize power dissipation regardless of the package used. To accommodate the option of using both 54 and 32 lead packages, the exposed pad PCB flag must be enlarged as shown in Figure 3

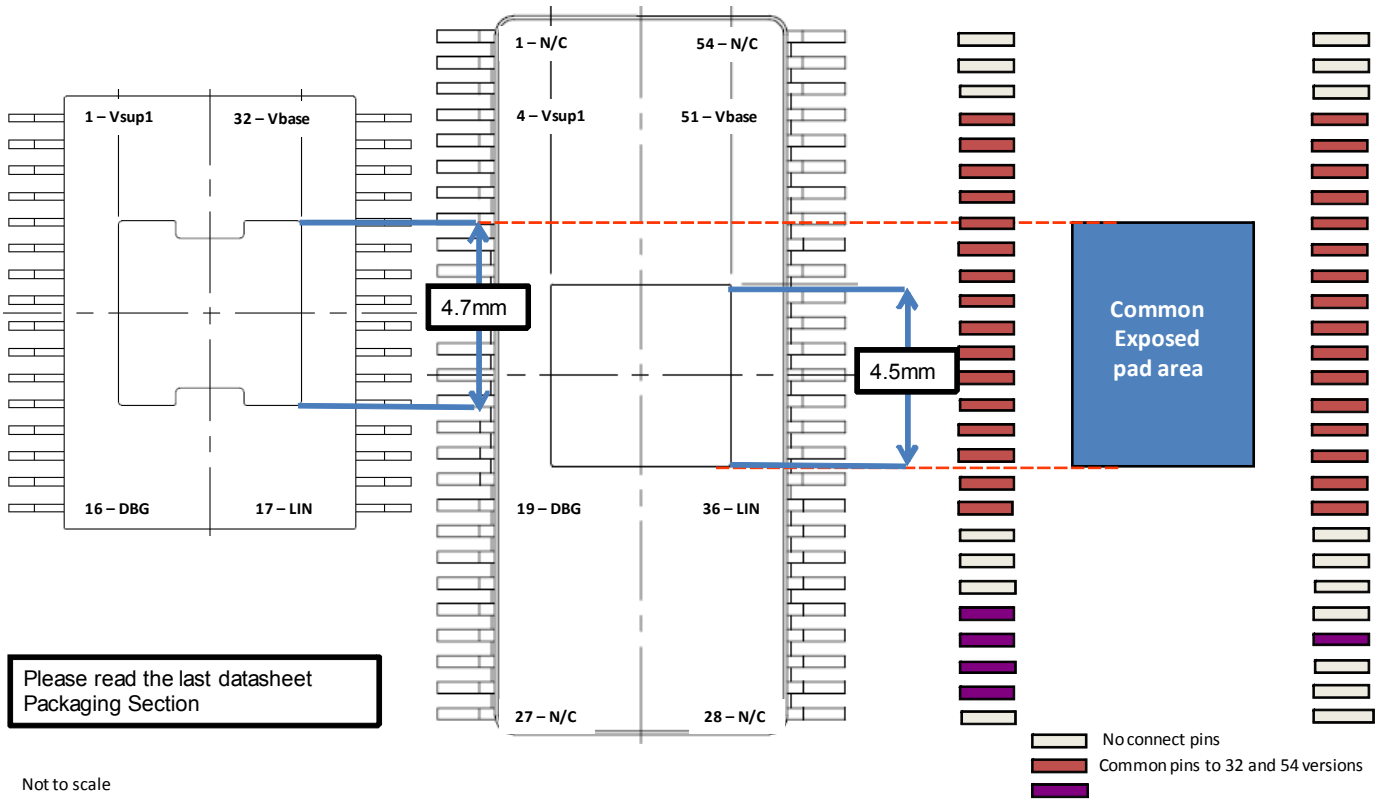
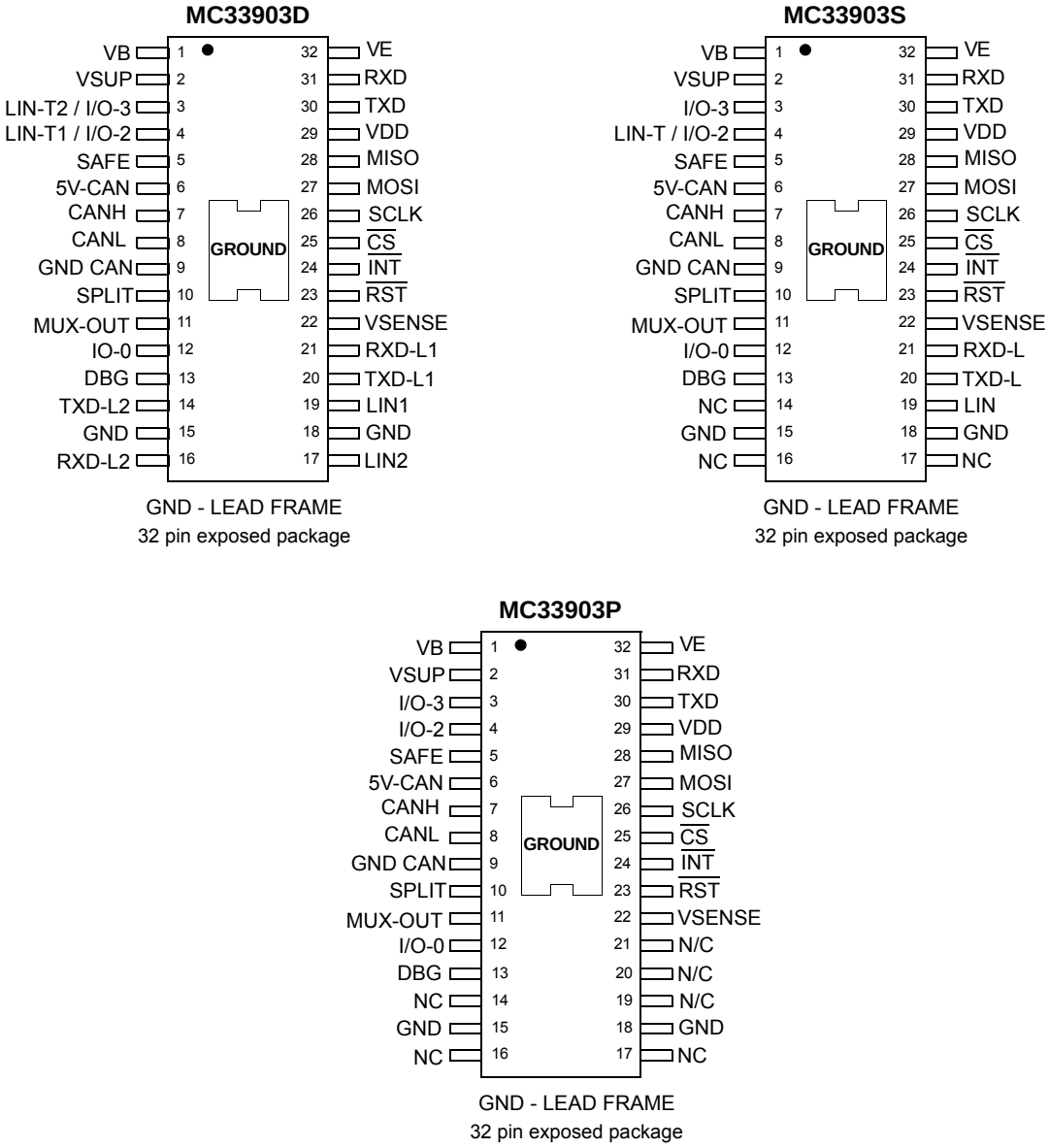


Figure 3. MC33905D, MC33905S, MC33904, and MC33903 exposed pad design

The other pin compatible group is made up of the MC33903D, MC33903S, and MC33903P as shown in Figure 4



Note: MC33903D, MC33903S, and MC33903P are footprint compatible.

Figure 4. MC33903D, MC33903S, and MC33903P pin compatibility

This group of pin compatible devices implements the same package so there is no need to accommodate the package placement or PCB exposed flag like the previously mentioned group.

2.3 Device identification

As previously described, there are numerous part numbers available to choose from and sometimes it may be difficult to keep track of which device has been mounted on a specific module. For this reason, the marking on a device is critical to understand. NXP has developed the SBC product numbering scheme shown in Figure 5.

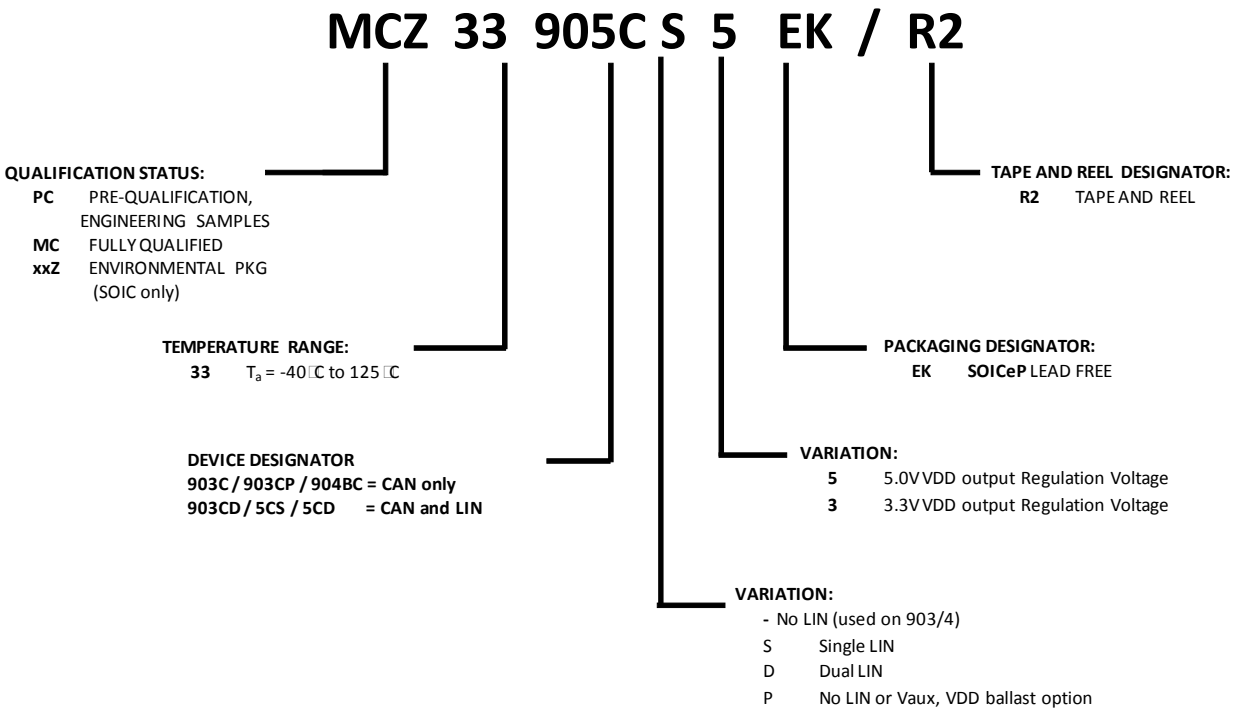


Figure 5. Device marking information

In addition to the physical marking on the device's package, the device's part number can also be acquired by the microcontroller via SPI communication by reading the assigned SAFE-INT register address (see Table 4). The SPI word that has to be sent on MOSI is 0x2580 and the corresponding data will be read on MISO by the microcontroller. This becomes extremely useful when the user does not have visual access to the physical device or the marking on the package has faded off.

Table 4. Device identification via SPI command

SAFE-INT Register							Device ID Coding				
00	1_0010 SAFE	1	1	V_{DD} (5.0 V or 3.3 V)	device p/n 1	device p/n 0	id4	id3	id2	id1	id0
Hexa SPI commands to get device Identification: MOSI 0x 2580 example: MISO bit [7-0] = 1011 0100: MC33904, 5.0 V version, silicon Rev. C (Pass 3.3)											

V_{DD} (5.0 V or 3.3 V)	Description	0: mean 3.3 V V_{DD} version 1: mean 5.0 V V_DD version
	Set / Reset condition	N/A
Device P/N1 and 0	Description	Describe the device part number: 00: MC33903 01: MC33904 10: MC33905S 11: MC333905D
	Set / Reset condition	N/A
Device id 4 to 0	Description	Describe the silicon revision number 10010: silicon revision A (Pass 3.1) 10011: silicon revision B (Pass 3.2) 10100: silicon revision C (Pass 3.3)
	Set / Reset condition	N/A

Note: This device identification feature is not available on the MC33903D, MC33903S, and MC33903P.

3 Device features

3.1 MC33903/4/5 functional blocks

SBCs may sometimes be perceived as complex devices that are hard to implement due to their extensive feature set, but working with these is actually quite simple. To design and develop a reliable and robust automotive application that implements the MC33903/4/5, the module designer must first have a good understanding of the SBC's features and circuit blocks functionality. **Figure 6** shows the internal block diagram for the MC33905D, which is the SBC with the most features compared to the rest of the SBC devices that also combine the necessary features to meet the designer's needs.

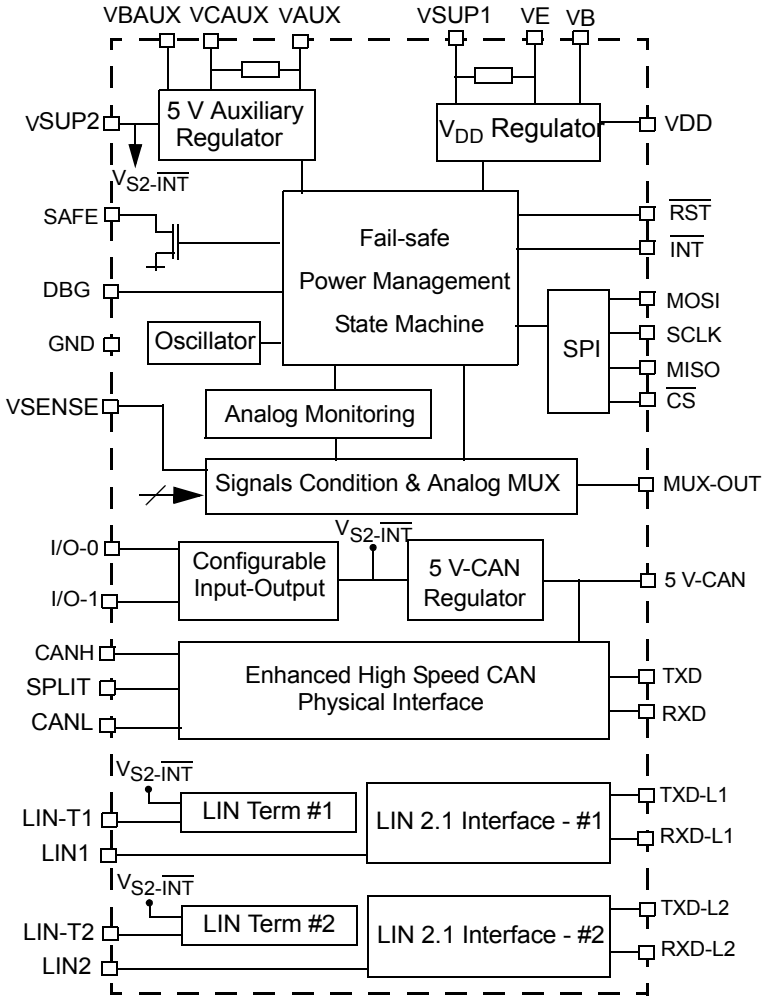


Figure 6. 33905D internal block diagram

3.1.1 Voltage supplies - VSUP1, VSUP2

This family of SBCs has been developed to meet rigorous 12 V automotive system requirements and with this in mind, it has two separate supplies. The purpose of having dual voltage supply inputs for some of these SBCs is to give the module designer the flexibility to use specific external components on the battery lines depending on module requirements. As shown in Figure 7, VSUP1 is a dedicated supply that feeds the main VDD regulator, which has the function of powering up the module's microcontroller. VSUP2 supplies V_{AUX}, 5V-CAN, LIN, and I/Os so in case of any faults on any of these, the VDD will not be affected due to its supply isolation.

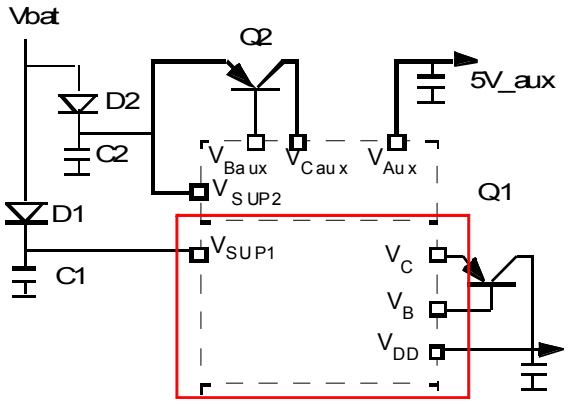


Figure 7. V_{SUP1} and V_{SUP2} Voltage supplies

In addition to the internal isolation of the V_{SUP1} to supply the VDD regulator feature, the module's designer can also optimize the external capacitor and reverse battery protection diode used on V_{SUP1} to sustain environmental conditions such as battery crank pulse and chattering.

The MC33903D, MC33903S, and MC33903P only have a single supply input (VSUP), which supplies VDD, VAUX, 5V-CAN, LIN, and I/Os. For these devices, VSUP1 and VSUP2 nodes are internally connected by wire bonds to the VSUP pin.

3.1.2 Voltage regulators - VDD, VAUX, 5V-CAN

There are two to three embedded voltage regulators included in the MC33903/4/5 SBC family. The VDD is the main regulator that supplies the microcontroller of the module. This regulator can be either 3.3 V or 5.0 V at +/-2% accuracy. The VDD voltage is dependent on part number. Refer to the data sheet for more details.

The Vaux regulator can also be 3.3 V or 5.0 V (at +/-5% accuracy), but in this case the voltage is configurable via SPI. Vaux is not implemented in all of the MC33903/4/5 SBC devices since some applications may not require this auxiliary regulator (see Table 1, Table 2, and Table 3).

The 5V-CAN regulator is a dedicated 5.0 V supply for the CAN physical layer. Ideally, this regulator should be used solely for the CAN interface, but some applications may not require this communication protocol. So for cases where there is no CAN transceiver implemented or during no CAN communication modes of the SBC, this regulator may also be used to supply another 5.0 V device. Good care must be taken to keep the device parametrically within specification (i.e. 5V-CAN current capability).

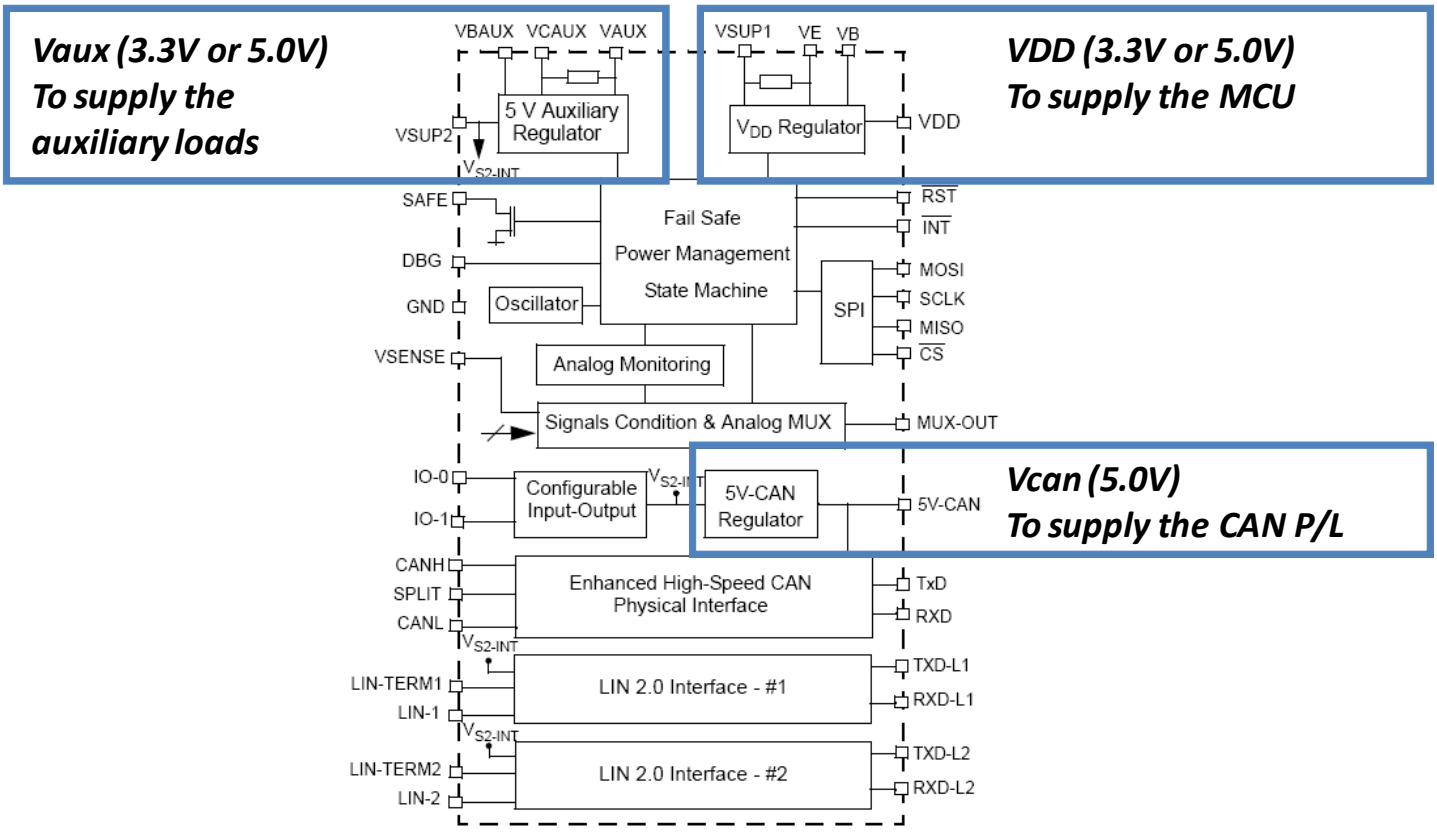


Figure 8. VDD, V_{AUX}, and 5V-CAN embedded regulators

3.1.3 Multiplexer - MUXOUT

The MC33903/4/5 family of SBCs implements an analog multiplexed output for some of the SBCs. The MUX-OUT pin should be connected to the analog to digital converter of the microcontroller. This output voltage is limited to the voltage on VDD and allows for the microcontroller to monitor critical environment conditions of the module such as V_{SUP}, V_{SENSE}, I/O-0, and I/O-1 voltages. Additionally, the SBC has an internal reference voltage of 2.5 V that can also be read on the MUX-OUT. The current sourced on VDD and the internal die temperature of the SBC can also be measured by the microcontroller by reading the MUX-OUT voltage.

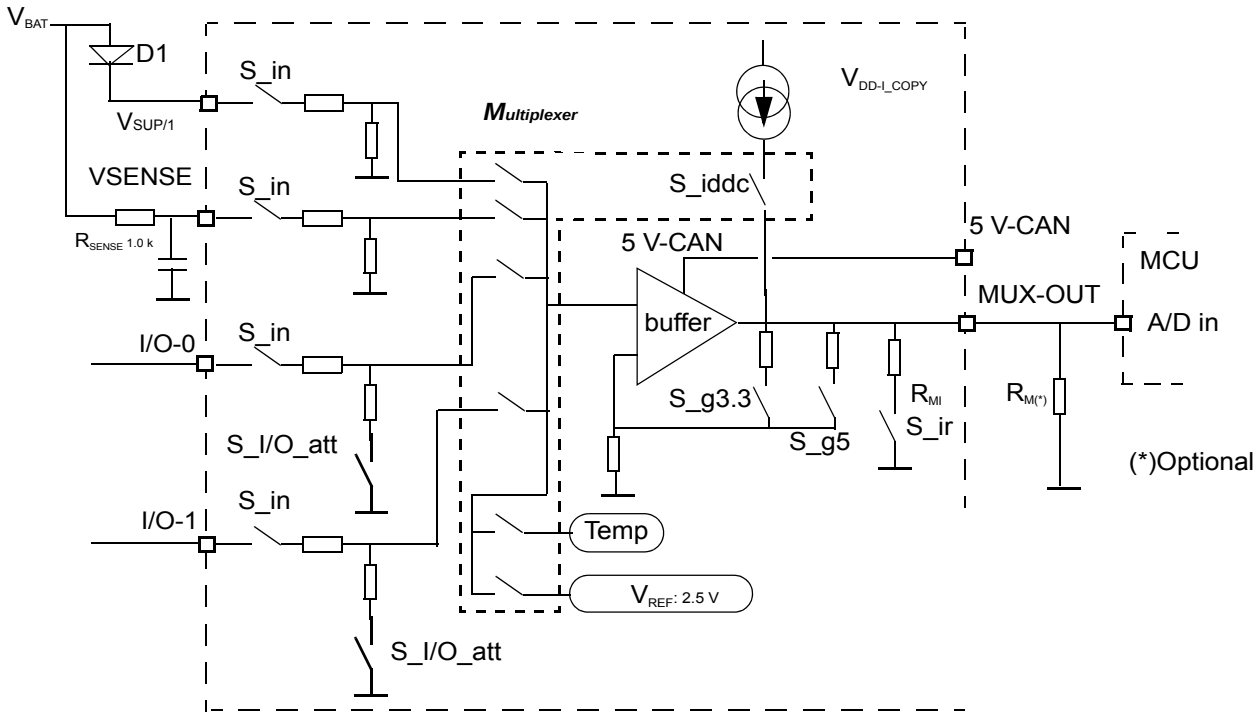


Figure 9. Multiplexer simplified internal diagram

The 5V-CAN voltage can be within the limits before or after V_{DD} voltage is available, and V_{DD} undervoltage reset is released.

Therefore it is recommended to validate the availability of the 5V-CAN voltage after a start-up of the device or return from an undervoltage condition, and before the MUX register write operation. This can be done with means of the flag 5V-CAN_UV in the Regulator Flag Register.

In addition to the dedicated 5V-CAN_UV, the 5V-CAN regulator undervoltage condition is also indicated by the bit VREG-G bit of the Fixed Status bits. Fixed Status is the first byte of each MISO frame. It is a good practice to implement an appropriate exception handling in the software, in case one or more of the Fixed Status bits are set.

Another possibility for verification of the MUX register is to read the register value back after a write operation. If the 5V-CAN regulator is OFF, a read-back of the MUX register (command 0x0100) returns the value 0x00.

3.1.4 Serial peripheral interface (SPI) - MOSI, MISO, SCLK, $\overline{CS}$

The 16 bit SPI communication in this family of SBCs has some unique features that can be implemented to improve the safety and robustness of the module's microcontroller and SBC interaction. There are 32 bit-addresses available for SPI communication and multiple types of watchdog operations can be implemented. Window watchdog is set by default and user can then select timeout or advanced watchdog thereafter.

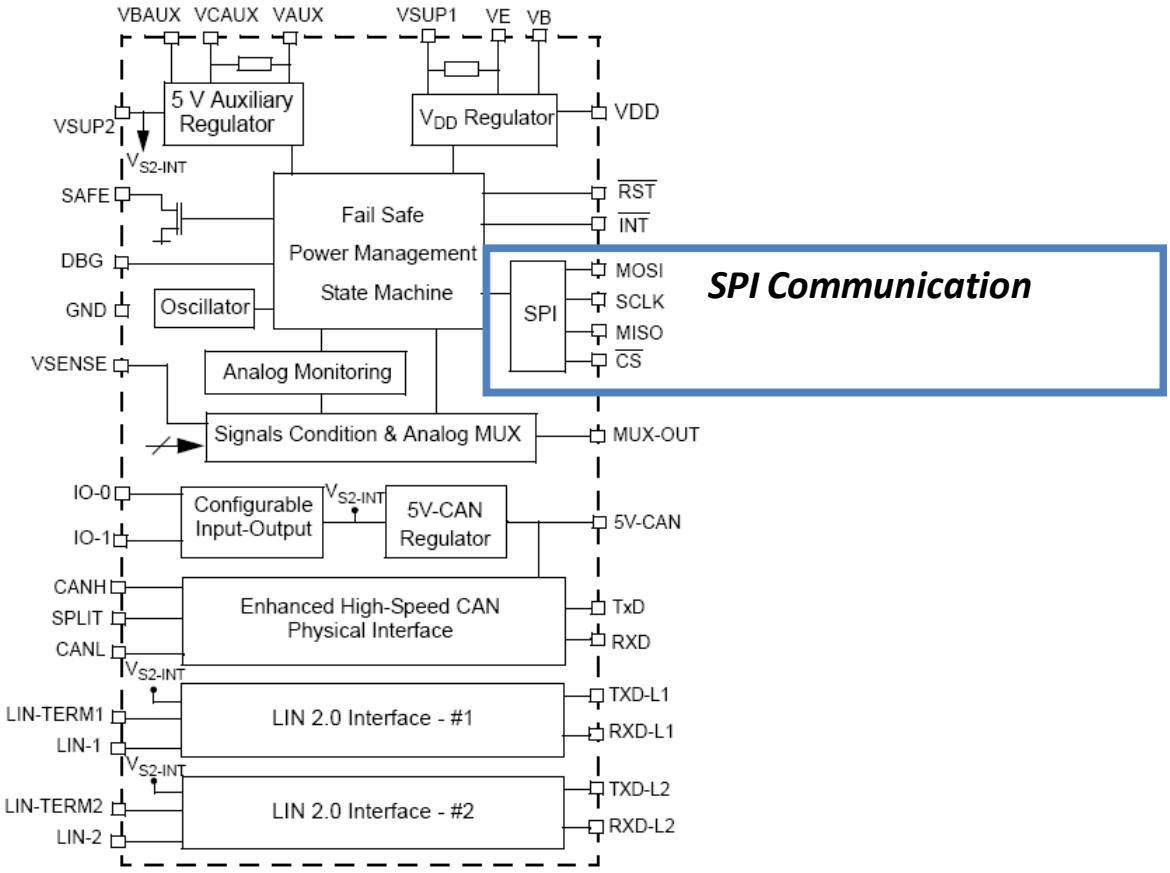


Figure 10. SPI port - MOSI, MISO, SCLK, and $\overline{CS}$

3.1.5 Configurable input/output - I/O-0, I/O-1, I/O-2, I/O-3

There are one to four configurable I/Os included in the MC33903/4/5 SBC family. These I/Os can be used to drive external transistors or small loads such as LED indicator lights. These I/Os can be configured as high-side or low-side outputs that switch to VSUP2 and GND correspondingly. Additionally, these can be configured as wake-up inputs, which can sustain automotive transients when connected to the battery line.

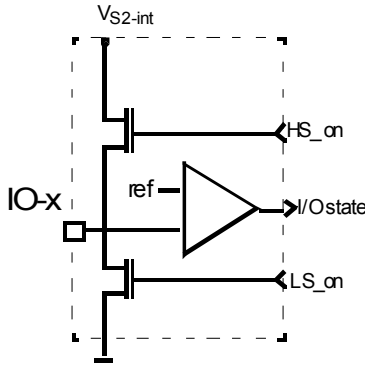


Figure 11. I/O simplified internal diagram

3.1.6 Safe modes - $\overline{\text{SAFE}}$, $\overline{\text{RST}}$, $\overline{\text{INT}}$

In addition to the continuous monitoring of the watchdog to maintain supervision of the microcontroller-SBC interaction, the SBC also features continuous monitoring of the battery voltage and the embedded regulators of the device. In case of serious module conditions due to faults on the battery resulting on VDD undervoltage conditions, a reset will be generated by the SBC.

There are also mask-able interrupts configurable to trigger upon CAN and LIN faults, overvoltage and undervoltage conditions on Vaux, 5V-CAN, V_{SUP}, and V_{SENSE}, missed watchdog/s, thermal issues and overcurrent conditions. Additionally, the microcontroller can voluntarily request and $\overline{\text{INT}}$ assertion by sending a SPI command.

The MC33903/4/5 family of SBCs also has a SAFE active-low output that is triggered in the event of a microcontroller failure, which could be indicated by multiple resets, RST pin shorted to GND, low VDD, or missed watchdog/s. The intention for this output signal is to drive electrical safe circuitry isolated from both the microcontroller and the SBC to put the module in a known state.

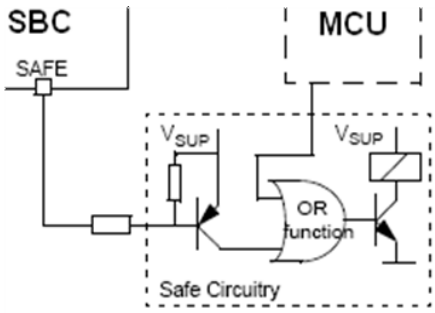


Figure 12. $\overline{\text{SAFE}}$ output typical application schematic

3.1.7 Physical layers - CAN & LIN

The MC33903/4/5 family of SBCs combines CAN and LIN physical layers with various features such as number of I/Os, number of regulators, multiplexing capability, etc. All devices have one CAN physical layer and dependent on part number, these may integrate one, two or no LIN transceivers.

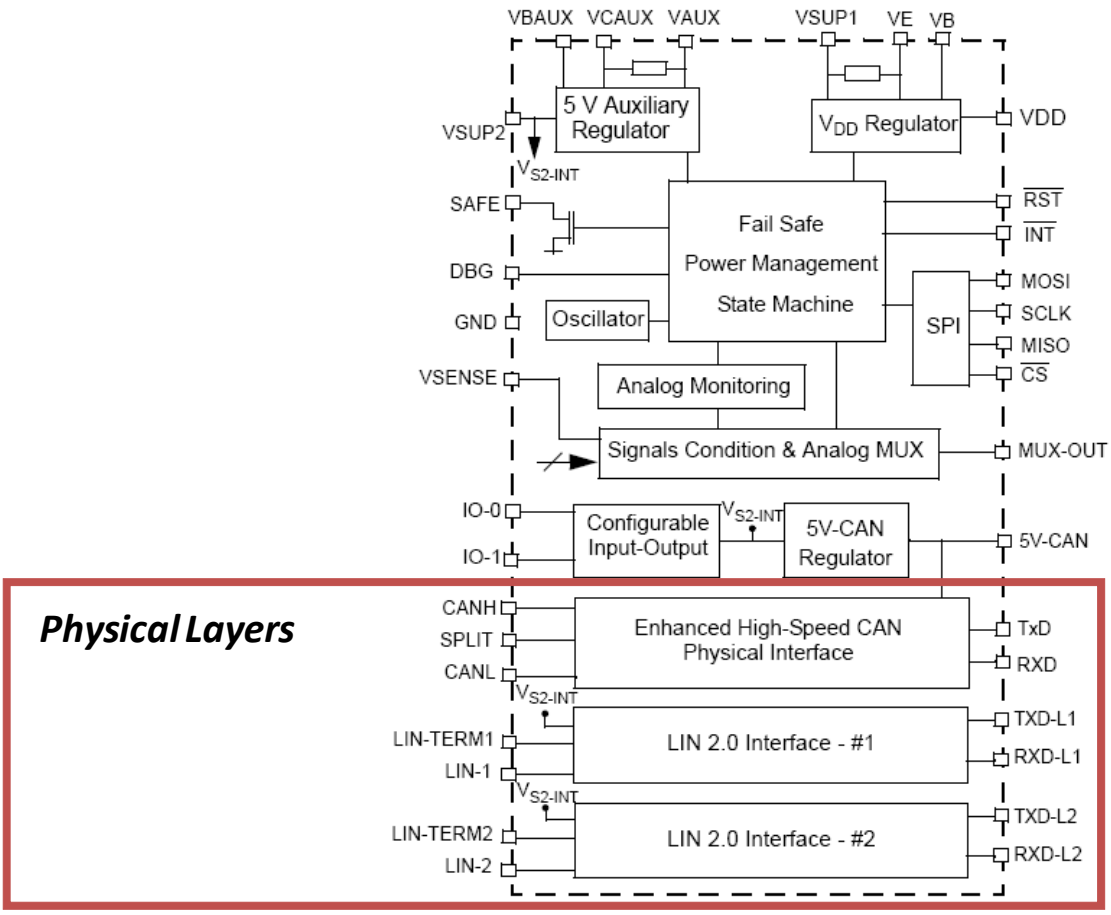


Figure 13. CAN and LIN physical layers

The CAN physical layer is fully compliant to ISO 11898-2 and ISO 11898-5 High Speed CAN protocol specifications. This allows for bus communication baud rates ranging from 40 kb/s up to 1.0 Mb/s via twisted pair.

The LIN physical layer is fully compliant to LIN 2.1 and SAE J2602-2 LIN protocol specifications, which allow single wire bus communication speeds of 20 Kb/s and 10.4 Kb/s correspondingly.

Both the CAN and LIN physical layers have been EMC/ESD certified by numerous worldwide OEMs. To accomplish this certification, the family of SBCs must be robust enough to conform to rigorous EMC/ESD tests that meet and exceed some of the OEM requirements.

4 Hardware design

Once the module designer has a good understanding of the SBC's features and circuit blocks functionality, a robust and reliable automotive module can then be designed. The typical application schematic, which is included in the datasheet, is a good starting point for the design and development of an automotive module that implements the MC33903/4/5.

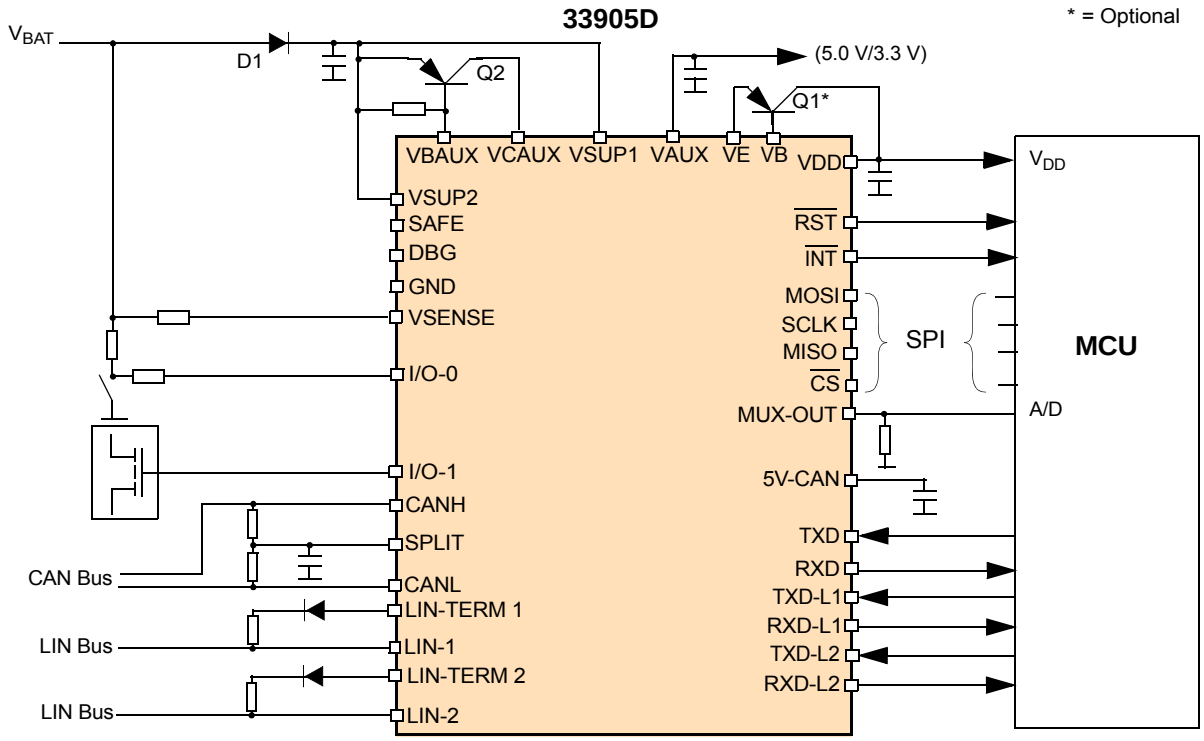


Figure 14. 33905D simplified application diagram

4.1 Supply environment

The automotive battery supply line is exposed to various high voltage transients, drops, and high/low frequency noise. To accommodate for this harsh supply environment, the MC33903/4/5 implements two separate supply lines for some of the SBCs and has a wide range of functionality depending on voltage of VSUP1 pin. Additionally, there is a VSENSE input that can optionally be connected directly to the battery through a 1.0 kΩ +/-1% resistor to monitor exact battery voltage via MUX-OUT. Figure 15 shows a typical way to connect the battery to all the supplies of the SBC. Note that the 22 µF capacitor on the V_{SUP} line is not required, but was implemented to test for CAN and LIN EMC per OEM's requirement of 10 µF minimum on the V_{SUP1} line.

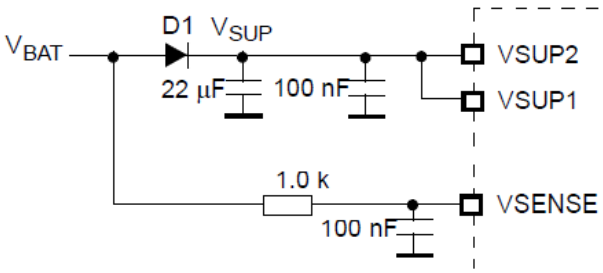


Figure 15. VSUP1 **and** VSUP2 **typical application schematic**

There are two options of connecting the SBC's voltage supply line to the car battery. One option is to short the VSUP1 and VSUP2 together and use the same protection and buffering external components (shown in Figure 16).

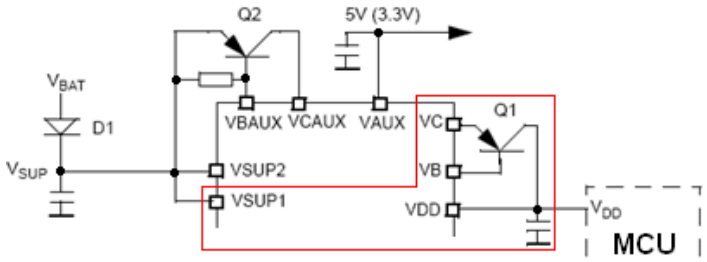


Figure 16. Single supply line typical application schematic

In this case, the same high voltage transients and drops will be seen on both VSUP1 and VSUP2. The module designer must also take into account that in addition to V_{AUX}, the V_{SUP2} line also supplies the 5V-CAN, LIN, and I/Os. Any perturbations on these circuit blocks affecting the V_{SUP2} supply line will also affect V_{SUP1} and perturb V_{DD} as a result.

The other option of connecting the supply lines is by separating V_{SUP1} and V_{SUP2} using different protection and buffering components as shown in Figure 17.

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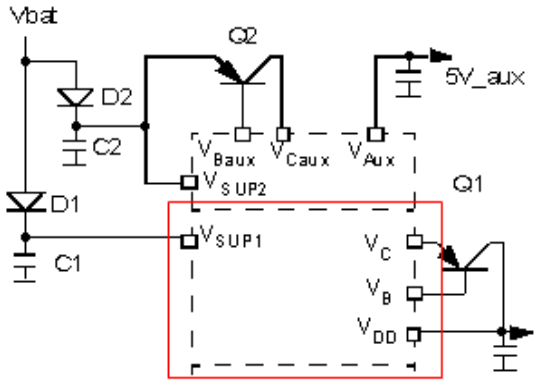


Figure 17. Separate supply lines typical application schematic

Although this adds some cost to the module's bill of material (BOM), in return it may prevent serious module malfunctions during extreme low battery conditions. Separating the supply lines allows for the optimization of the buffering capacitor for handling automotive conditions such as cranking, battery chattering and others. Additionally, a conventional reverse battery protection diode can be replaced with a Schottky type to further decrease the voltage drop from battery to VSUP1. This will give VDD more headroom to stay above the minimum voltage threshold and keep the microcontroller fully functional.

Optionally, VSENSE can be connected directly to the car's battery through a 1.0 kΩ +/-1% resistor to acquire exact battery voltage and deliver it to the microcontroller via MUX-OUT. The high accuracy of the resistor is required to keep the MUX-OUT reading at +/-1% accuracy. If battery voltage accuracy reading is not required, lower accuracy resistors can also be used (1.3 kΩ resistor on VSENSE will change the MUX-OUT ratio by about 1%; 10 kΩ will change ratio by about 7%). Note that although the MC33903/4/5 family of SBCs maximum nominal voltage is 28 V, the VSENSE reading out on MUX-OUT will only cover 5.5 V to 27 V.

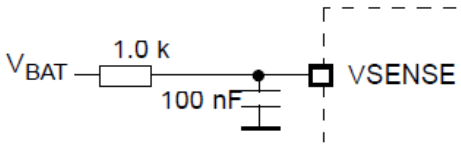
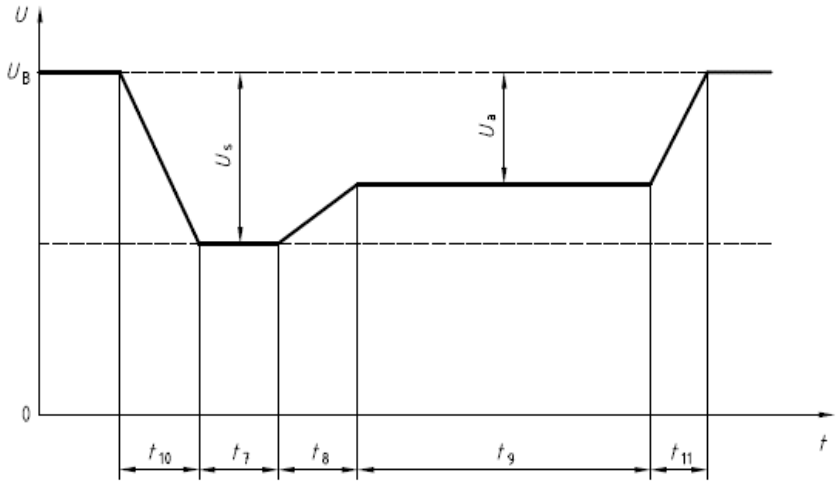


Figure 18. VSENSE typical application schematic

4.1.1 Crank pulse and battery chattering

OEMs require that modules withstand various pulses on the supply line, some of which are part of the ISO 7637 specification. Pulse 4 of the ISO 7637 emulates the battery line voltage transitions during engine start (see Figure 19). The MC33903/4/5 is able to function properly during these voltage dips and even lower voltages than the worst case conditions incorporating enhanced diagnostics and keeping the module's microcontroller running.



Parameter	12 V system
U_s	– 6 V to – 7 V
U_a	– 2,5 V to – 6 V with $\lvert U_a \rvert \leqslant \lvert U_s \rvert$
t_7	15 ms to 40 ms
t_8	$\leqslant$ 50 ms
t_9	0,5 s to 20 s
t_{10}	5 ms
t_{11}	5 ms to 100 ms

Figure 19. Crank pulse parameters

Taking the worst case conditions for pulse 4, as specified on the ISO 7637, results in the voltage waveform shown in Figure 20 for the battery line (represented by Vbat [in green] in Figure 21).

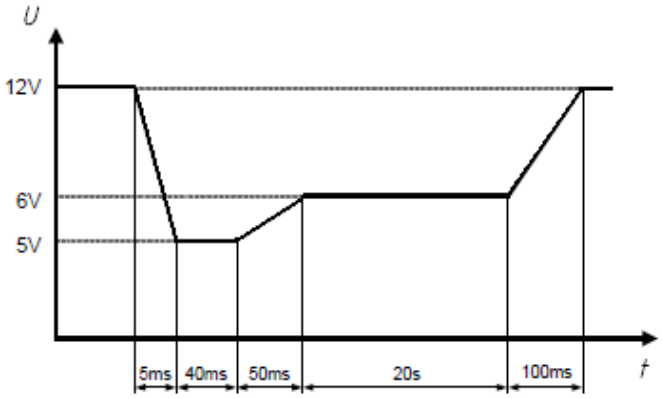


Figure 20. Worst case crank pulse

Figure 21 shows all the various transitions of the key voltages of the module during the crank pulse on battery voltage and how these are handled by the MC33903/4/5 (5.0 V V_{DD} devices). Note that a Schottky diode is not required to withstand these pulse conditions. As the battery voltage decreases, the SBC can immediately acknowledge this via the VSENSE input, which is directly connected to the battery through a 1.0 kΩ +/-1% resistor. A flag will be set when VSENSE voltage reaches ~8.6 V and can be configured to generate an interrupt or mask it for the microcontroller. Due to the capacitor on the VSUP line, its voltage will decrease at a slower rate and when it reaches ~6.0 V, a flag is set and the SBC can also optionally be configured to generate an interrupt or mask it for the microcontroller. As the V_{SUP} voltage continues to decrease, the V_{DD} voltage eventually tracks it with typically ~200 mV drop. VDD can be configured to generate a RST and/or INT (maskable) at 4.6 V or down to 3.2 V.

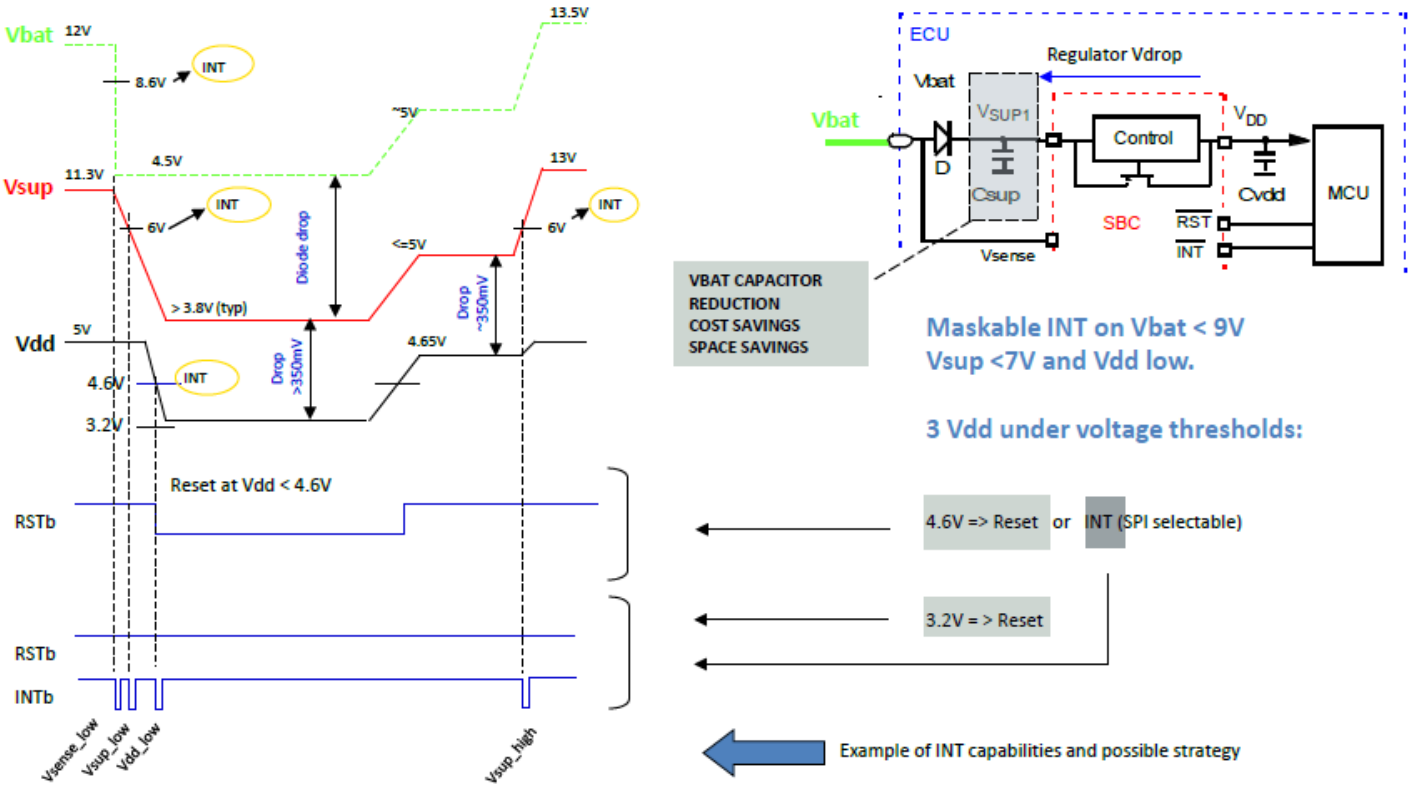


Figure 21. Crank pulse handled MC33903/4/5

As battery voltage starts to increase, V_{SUP} tracks it and V_{DD} tracks V_{SUP}. When V_{DD} reaches 4.6 V, RST is released and the microcontroller can function accordingly. When the V_{SUP} reaches ~6.0 V, an interrupt can be generated depending on SBC configuration.

All these capabilities of the MC33903/4/5 allow the engineer to implement highly intelligent modules with enhanced diagnostics. These modules are capable of sustaining aggressive conditions such as pulse 4 of the ISO 7637 as well as battery chattering without the need for higher cost capacitors and/or Schottky diodes. This doesn't only reduce cost, but also optimizes PCB real estate.

In addition to low battery conditions, the MC33903/4/5 will also withstand higher than nominal voltage conditions/pulses on the battery line such as 40 V Load Dump (pulse 5b of ISO 7637). Figure 22 shows all the voltage ranges the SBC can handle and what functionality can be expected during these voltage ranges. Shown in blue are the flags that will automatically be set for the microcontroller to acknowledge.

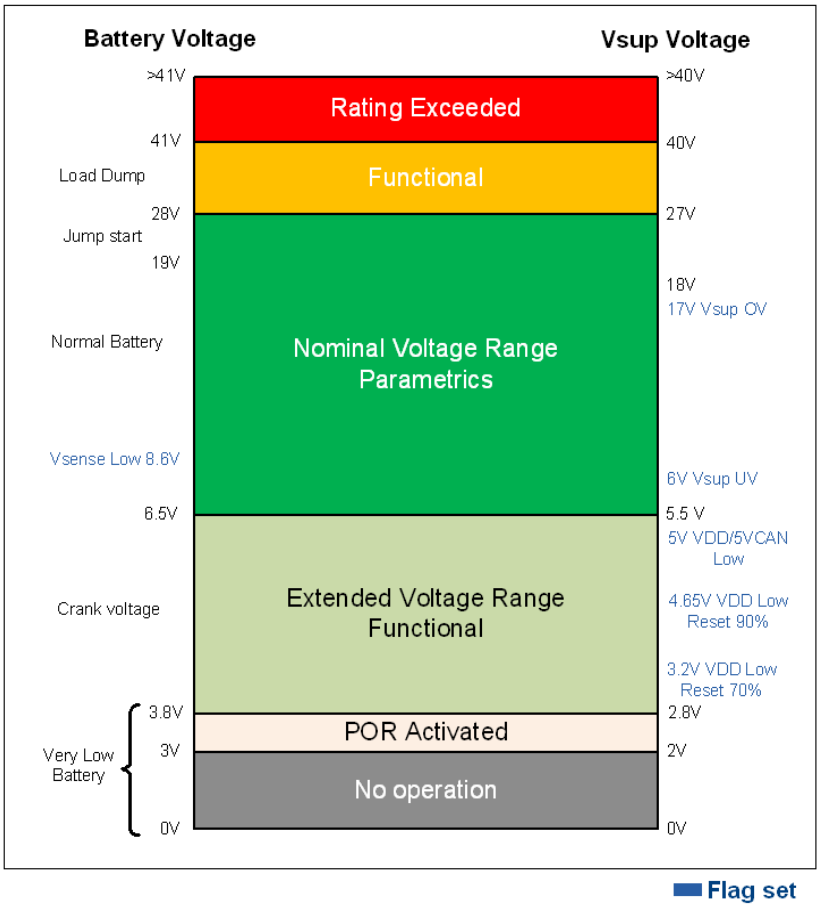


Figure 22. Supply voltage ratings

4.1.2 V_{SUP} ramp up slew rate

Note: The following recommendation does not apply to the D version.

V_{DD} regulator is connected to V_{SUP}. V_{DD} regulator start up could be influenced by V_{SUP} ramp up slew rate at low temperatures.

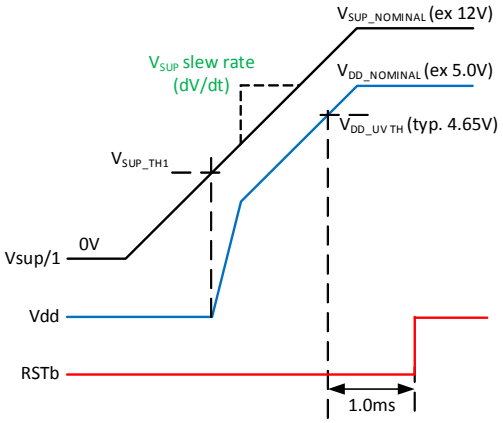


Figure 23. V_{SUP} dV/dt limit

Both behaviors described below could be observed on specific application where V_{SUP} is switched on and off with front relay and regularly generates this specific dV/dt. The behavior is not observed in typical applications where V_{SUP} is directly connected to the battery.

These behaviors depend on V_{SUP} slope at start-up, V_{SUP} voltage and temperature. Two different conditions have been identified:

- No V_{DD} SSR (Slow Slew Rate on V_{SUP})
- No V_{DD} FSR (Fast Slow Rate on V_{SUP})

4.1.2.1 No V_{DD} SSR

V_{DD} case 2, as described in Figure 23, has been observed with following conditions:

- V_{SUP}-min = 1.0 V
- V_{SUP} nominal = 9.0 V
- Cold temperature conditions: from 5.0 °C to –40 °C
- V_{SUP} slow slew rate: 10 mV/ms

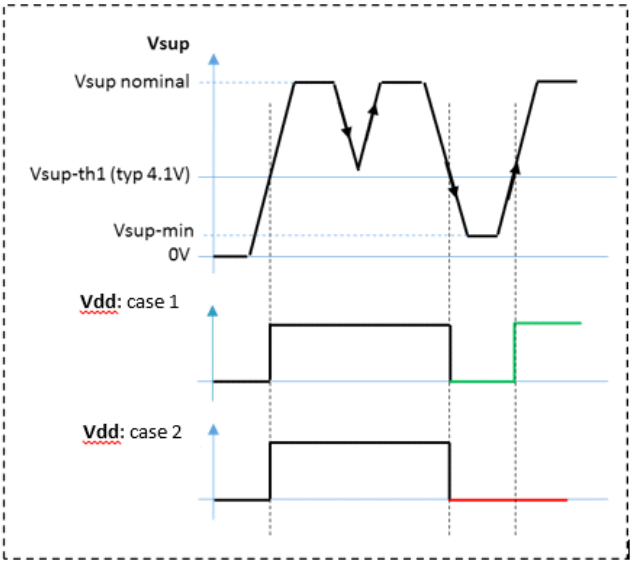


Figure 24. Slow slew rate on V_{SUP}

4.1.2.2 No V_{DD} FSR

V_{DD} case 2, as described in Figure 24, could be observed if all following conditions are met:

- V_{SUP} slew rate is faster than 10 mV/µs
- Cold temperature from 0 °C to –40 °C

Risk assessment:

- 0 ppm is dV/dt slower than 10 mV/µs
- 0.33 ppm to 50.3 ppm with 90% confident Level, if dV/dt is faster than 10 mV/µs
- 0.66 ppm to 42.8 ppm with 60% confident level, if dV/dt is faster than 10 mV/µs

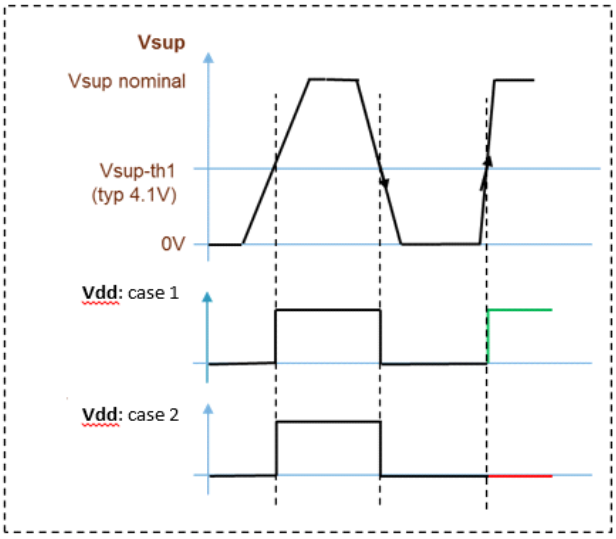


Figure 25. Fast slew rate on V_{SUP}

The V_{SUP} ramp up slew rate and voltage level should be controlled as described below, especially in applications where V_{SUP} switches on and off regularly.

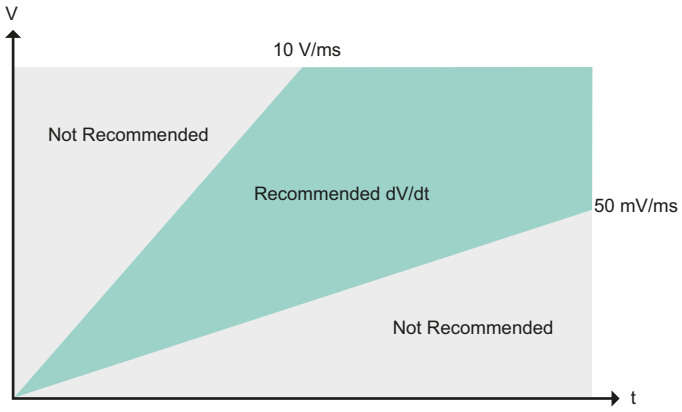


Figure 26. V_{DD} start up versus V_{SUP}/1 ramp

4.2 Regulators

The MC33903/4/5 offers three low dropout linear voltage regulators. V_{DD} is specifically supplied by VSUP1 separately from VAUX and 5V-CAN, which are supplied by VSUP2. Some buffering capacitors have to be implemented on the regulators depending on application. There is also the option to increase the current capability of the VDD regulator by implementing an external ballast transistor. The MC33903D, MC33903S, and MC33903P only have one supply input (V_{SUP}), which supplies all three regulators. For these devices, V_{SUP1} and V_{SUP2} nodes are internally connected by wire bonds to the VSUP pin.

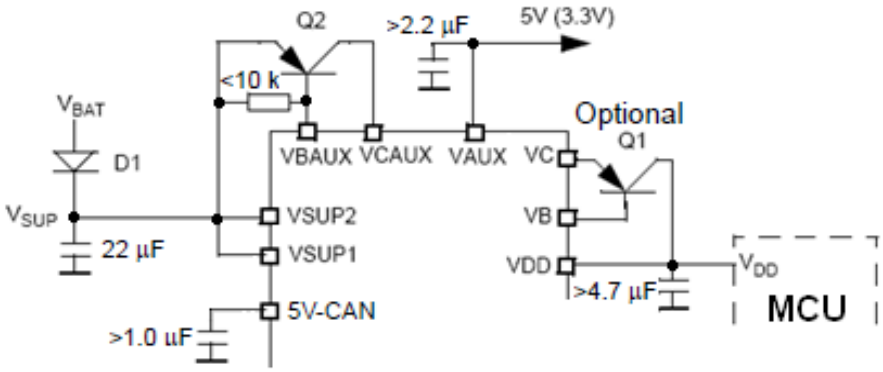


Figure 27. VDD, VAUX, and 5V-CAN typical application schematic

4.2.1 VDD

Supplying the microcontroller, VDD is the main regulator for the module. All MC33903/4/5 SBCs are available with 5.0 V or 3.3 V VDD (part number selectable). The current capability and voltage monitoring of this regulator is critical for the application. There are various safety features integrated into this regulator allowing for a highly robust and smart module design. VDD has overcurrent, overtemperature, and undervoltage detection. In case of overtemperature, the regulator will turn off automatically to protect itself from damage. The SBC is continuously monitoring the VDD voltage and will trigger an interrupt or reset during undervoltage conditions.

Figure 28. V_{DD} typical application schematic options

VDD does not require any discrete components other than a minimum of 4.7 µF capacitor. Optionally, VDD's 150 mA current capability can be increase by the implementation of an external PNP bi-polar junction transistor. When the transistor is not implemented, VC and VB pins must be left open. When the PNP transistor is implemented, 1/3 of the current will flow through the device and 2/3 will flow outside through the external ballast transistor. The recommended PNP bi-polar junction transistors are MJD42C and BCP52-16.

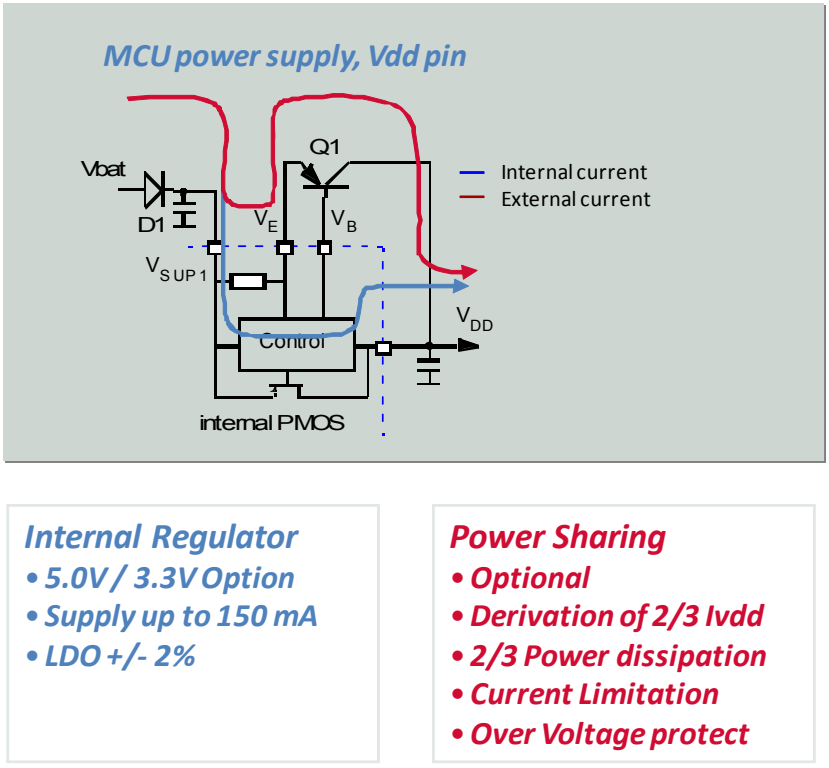


Figure 29. VDD power sharing capability

4.2.2 VAUX

The VAUX regulator can be used to supply other ICs such as switch detection interfaces, standalone CAN transceivers, RF modules, back up microcontroller, etc. This 5.0 V or 3.3 V +/-5% accuracy auxiliary regulator is available on all MC33904/5 SBCs, except the MC33903. The V_{AUX} output voltage level is selectable by the SPI during the SBC's initialization phase (default is 3.3 V). This regulator has overcurrent and undervoltage detection and automatic shutdown for protection. Additionally, the SBC can be configured to trigger an interrupt for the microcontroller in case of an overcurrent or undervoltage condition.

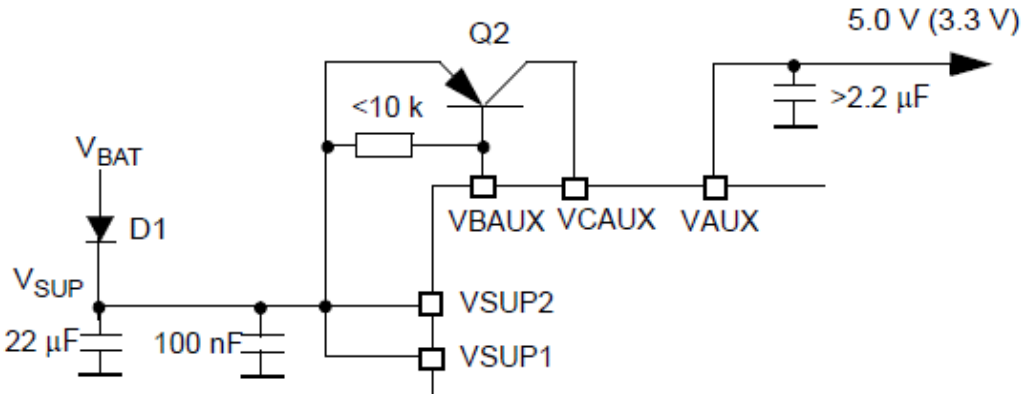


Figure 30. V_{AUX} typical application schematic

This regulator requires an external PNP bi-polar junction transistor, a resistor, and a buffering capacitor, as shown in Figure 30. The transistor enables better power dissipation to enhance the current capability of V_{AUX} (MAX: 250 mA). This regulator is OFF by default and controlled by SPI after power-up. The recommended PNP bi-polar junction transistors are MJD42C and BCP52-16.

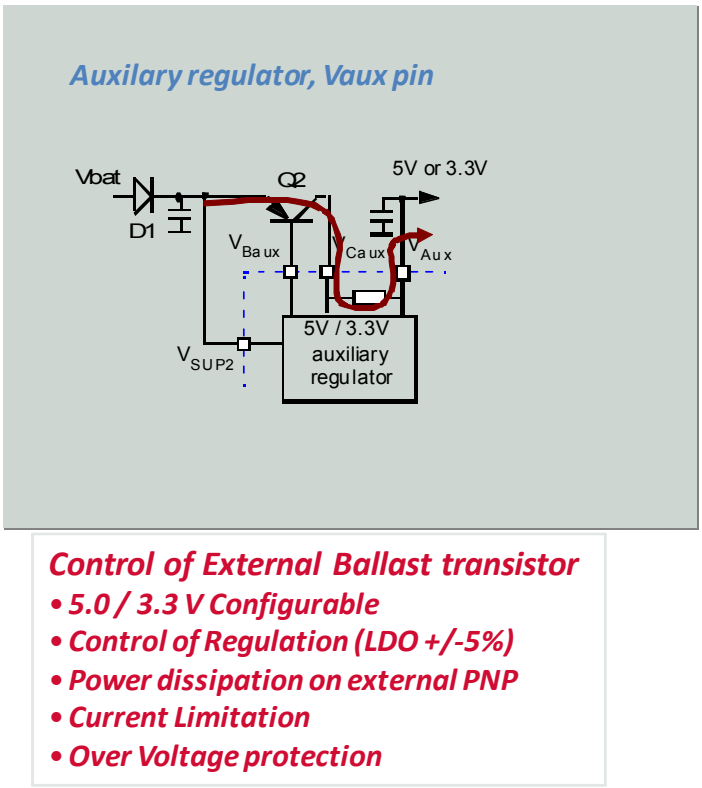


Figure 31. V_{AUX} nominal application characteristics

4.2.2.1 Extending current capability and routing outside of module

If more than 250 mA of current capability is required out of the V_{AUX} regulator, it is possible to extend the current capability by implementing a non-typical use case for the SBC (see Figure 32). Be warned that when using the SBC as described, the V_{AUX} internal current limitation is deactivated. In this case, the current will be limited by the VBAUX drive capability. Using the recommended transistors MJD42C or BCP52-16 will increase the V_{AUX} MAX current capability to 500 mA (considering a DC gain greater than 25).

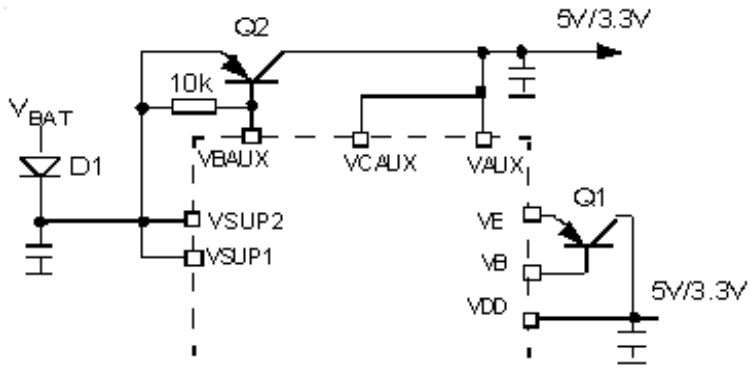


Figure 32. V_{AUX} increased current capability without current limit schematic

If current limit is required with higher MAX current capability, it is possible to accomplish this with a few additional components as shown in Figure 33. In this case, the external current limit will be V_{BE} of Q3 divided by Rs. The recommended PNP bi-polar junction transistors are MJD42C and BCP52-16.

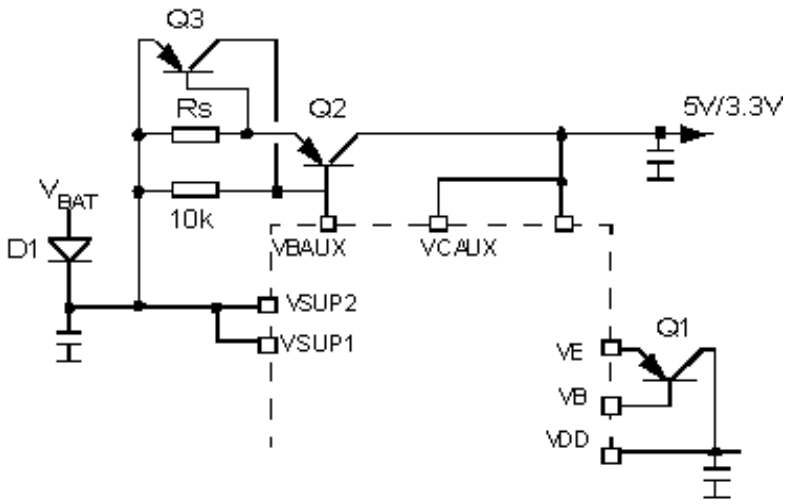


Figure 33. V_{AUX} increased current capability with external current limit schematic

Some applications require that the V_{AUX} regulator be brought outside of the module. This option is also available for the MC33904/5 SBCs with some limitations by implementing a few additional components. Adding a 5.2 V zener diode and a 100 Ω resistor as shown in Figure 34, will allow V_{AUX} to survive shorts to +20 V. Be warned that by implementing this circuitry, the current limit function is disabled. The V_{AUX} voltage will also increase by about 40 mV compared to the internal typical use case voltage shown in Figure 30. The recommended PNP bipolar junction transistors are MJD42C and BCP52-16.

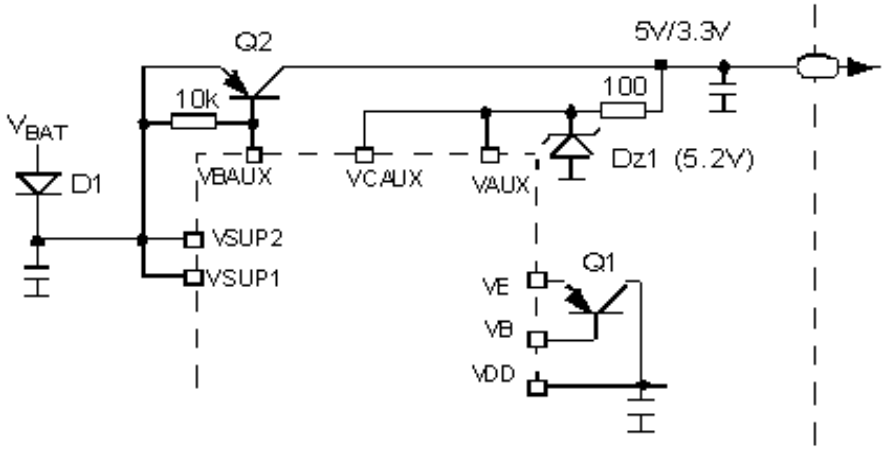


Figure 34. V_{AUX} routed outside module with +20 V protection and without current limit

If current limit is required with higher MAX current capability and V_{AUX} needs to go outside the module, it is possible to accomplish this with a few additional components as shown in Figure 35. Adding a 5.2 V zener diode and a 100 Ω resistor will allow V_{AUX} to survive shorts to +20 V. In this case, the external current limit will be Vbe of Q3 divided by Rs so the SBC will also survive shorts to GND. The V_{AUX} voltage will increase by about 40 mV compared to the internal typical use case voltage shown in Figure 30. The recommended PNP bi-polar junction transistors are MJD42C and BCP52-16.

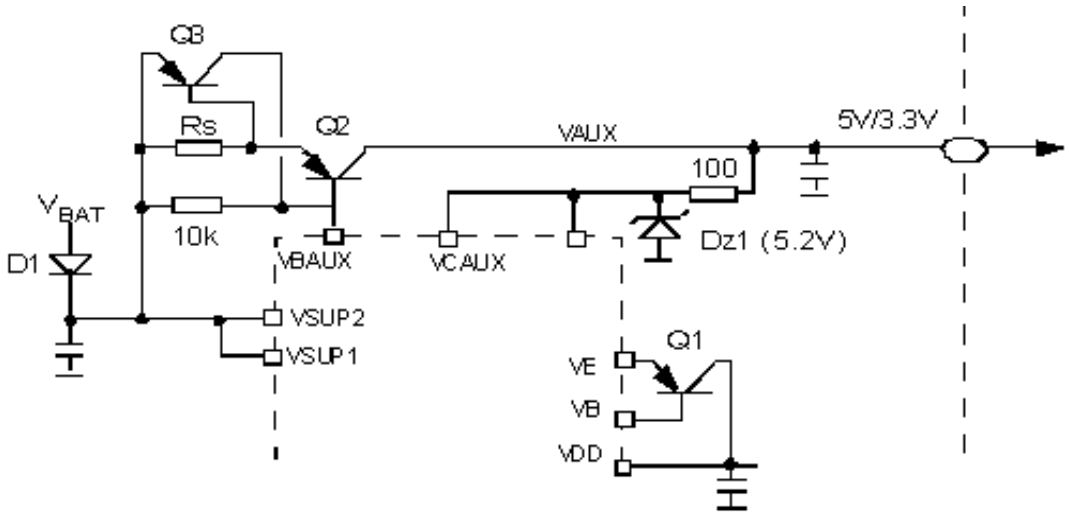


Figure 35. V_{AUX} routed outside module with +20 V protection and external current limit

If it's required for the V_{AUX} to be brought outside the module and to handle positive transient voltages up to +40 V (Load Dump), this can be accomplished by adding a few additional components. Be warned that the V_{AUX} current limit will be disabled and the voltage drop will be higher due to the diode drop of D2 shown in Figure 36. Short to GND detection can be done via the V_{AUX} undervoltage detection. The recommended PNP bi-polar junction transistors are MJD42C and BCP52-16.

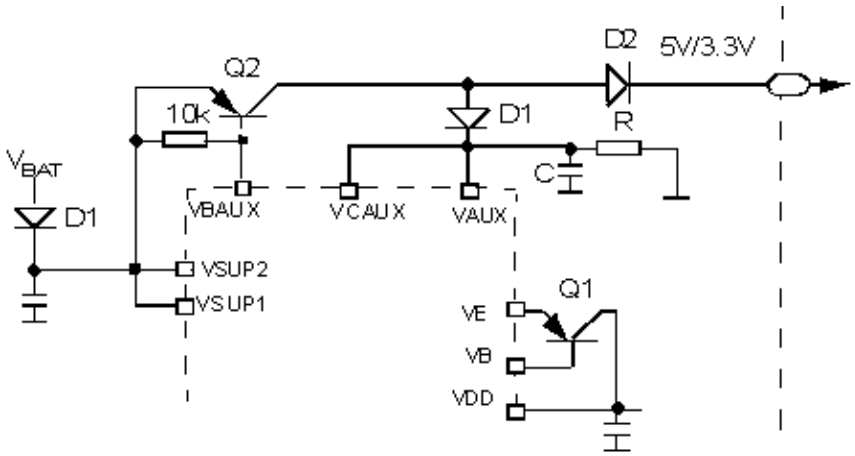


Figure 36. V_{AUX} routed outside module with +40 V protection and without current limit

4.2.3 5V-CAN

The 5V-CAN is a dedicated 5.0 V +/-5% accuracy regulator to supply the CAN interface of the MC33903/4/5 SBC family. This regulator has overcurrent, overtemperature, and undervoltage detection and automatic shutdown for protection. It requires a minimum of 1.0 µF buffering capacitor and typically nothing else is connected to this regulator as shown in Figure 37. MUX-OUT and some blocks of the LIN interfaces are also powered by the 5V-CAN. In order to have a functional multiplexer and the LIN interfaces operational in transmit/receive mode, the 5V-CAN must be ON. This regulator is OFF by default and must be turned ON via the SPI. Note that when in debug mode, 5V-CAN is ON by default.

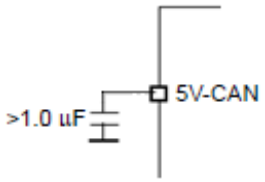


Figure 37. 5V-CAN typical application schematic

Although it is possible to supply other ICs with this regulator, it is not recommended mainly due to EMC performance degradation. In such cases, module designer must take good care to keep the SBC within specification. Some applications may not require CAN communication making the use of the 5V-CAN to supply other devices on the module more feasible. Optionally, this regulator may also supply other devices during non-CAN communication modes of the SBC.

4.3 Multiplexer

Some of the devices that are part of the MC33903/4/5 SBC family include an analog multiplexer to connect to the module's microcontroller A/D converter. Critical environment conditions such as: V_{SUP1}, V_{SENSE}, I/O-0, I/O-1, internal 2.5 V V_{REF}, die Temp, and V_{DD-I} current copy can be monitored. The output voltage on MUX-OUT is limited to the voltage on VDD. This allows the microcontroller to gather critical module data and react accordingly to enhance the safety of the system.

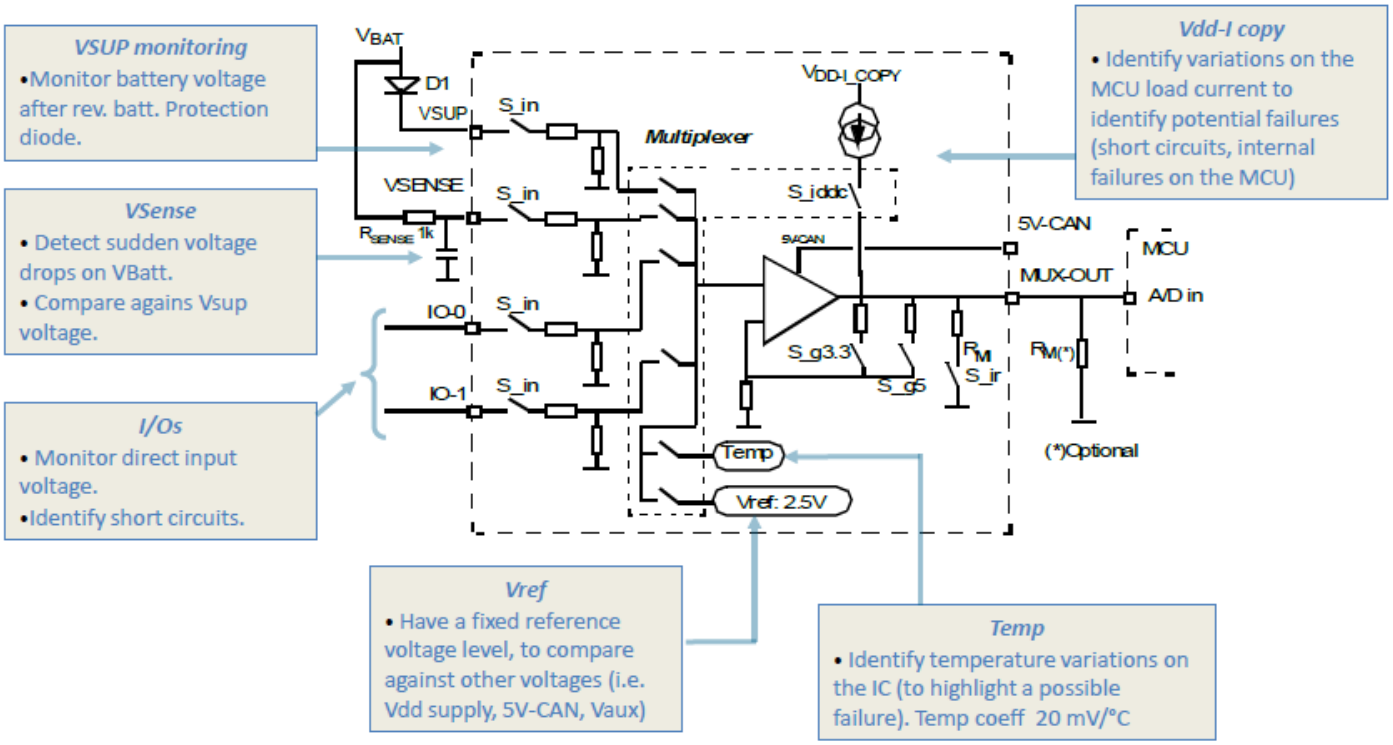


Figure 38. Multiplexer monitoring capabilities

There are no additional components required to access the MUX-OUT since it can be connected directly to the microcontroller except for applications where the VDD current has to be monitored. In this case, a resistor from MUX-OUT to GND is required. An external 2.0 kΩ or greater resistor is recommended (see Figure 39). Optionally, an internal resistor can be activated via the SPI, but the resistance variation is much greater than implementing an external one. As a result, implementing an external resistance will give more accurate readings on the MUX-OUT.

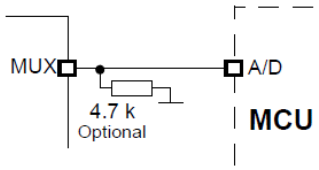


Figure 39. Multiplexer typical application schematic

Note: Although the MC33903/4/5 family of SBCs maximum nominal voltage is 28 V, the VSENSE reading out on MUX-OUT will only cover 5.5 V to 27 V.

4.4 SPI communication

The main communication between the microcontroller and the MC33903/4/5 is through the SPI port, which is made up of MOSI, MISO, SCLK, and $\overline{CS}$. The maximum frequency of the SBC's 16-bit SPI is 4.0 MHz and there are 32 bit-addresses available. The logic voltage level of the SBC's SPI port will be determined by the V_{DD} voltage, which supplies the microcontroller. There are no additional components required for the SPI port circuitry, but series resistor footprints are recommended on all SPI pins (see Figure 40) in case of aggressive noise immunity requirements. If this is not an issue, these can be populated with 0 Ω resistors. Note that the series resistance should not exceed 1.0 kΩ because this may cause some degradation on the signals due to the parasitic capacitance and dependency on the communication speed.

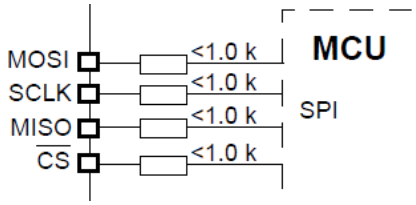


Figure 40. SPI typical application schematic

Note: The MC33903/4/5 SBC family does not allow for SPI daisy chain implementation

4.5 Configurable I/Os and LIN-terminations

The MC33903/4/5 family of SBCs offers one to four configurable I/Os and zero to two LIN-Ts dependent on part number (see Table 1, Table 2, and Table 3). These are all rated to withstand -0.6 V up to +40 V (Load Dump) and can be configured as outputs or wake-up inputs. When configured as outputs, these can be used to drive small loads as a high-side switch or a low-side switch with thermal protection in case of overload conditions. These can also be set to high-impedance for lower module current consumption when not in use.

4.5.1 I/O-0 and I/O-1

I/O-0 and I/O-1 are configured as wake-up inputs by default and the configuration state can be read via the SPI. The SBC will wake-up on both a 'high' to 'low' or 'low' to 'high' transition. I/Os can be configured to continuously monitor for transitions or 'cyclic sense wake-up' can be implemented on I/O-1 to decrease module current consumption.

Table 5. I/O-0 and I/O-1 functionality

I/O	WU Input	High-side	Low-side
0	yes	20 mA	0.4 mA
1	yes	0.4 mA	0.4 mA

A 22 kΩ resistor and a 100 nF decoupling capacitor are required for wake-up input implementation. R_{BAT} (10 kΩ recommended) is user defined depending on module current consumption requirements since it may potentially be connected to battery permanently (See Figure 41).

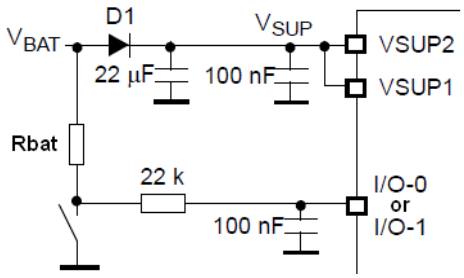


Figure 41. I/O-0 and I/O-1 input typical application schematic

When I/O-0 and I/O-1 are configured as outputs, these can be either high-side or low-side switches. When configured as a high-side, the output will be switched to V_{SUP2} voltage. When configured as a low-side, the output will be switched to GND. The R resistor shown on the I/O in Table 42 is not required, but it is recommended to improve ESD performance and its value will be dependent on the circuitry the I/O has to drive.

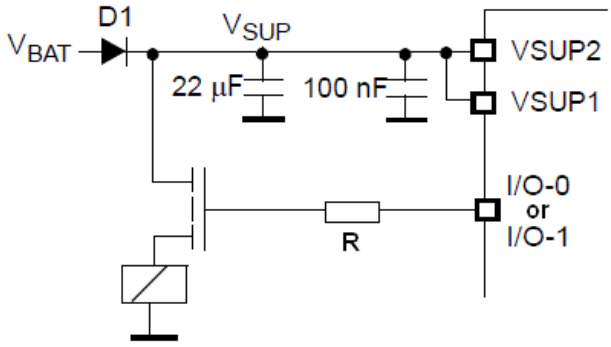


Figure 42. I/O-0 and I/O-1 output typical application schematic

The value of resistor R will also be determined by taking into account the maximum current capability of the I/O. Look at Table 5 for high-side and low-side current capability for I/O-0 and I/O-1.

4.5.2 I/O-2 and I/O-3

I/O-2 and I/O-3 are disabled by default and must be configured by SPI during SBC initialization. When configured as wake-up inputs, the SBC will wake-up on both a 'high' to 'low' or 'low' to 'high' transition. These I/Os can be configured to continuously monitor for transitions or 'cyclic sense wake-up' can be implemented on I/O-2 and I/O-3 to decrease module current consumption.

Table 6. I/O-2 and I/O-3 functionality

I/O	WU input	High-side	Low-side
2	yes	20 mA	N/A
3	yes	20 mA	N/A

A 22 kΩ resistor and a 100 nF decoupling capacitor are required for wake-up input implementation. R_{BAT} (10 kΩ recommended) is user defined depending on module current consumption requirements since it may potentially be connected to battery permanently (See Figure 43).

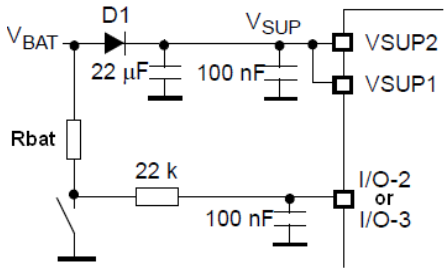


Figure 43. I/O-2 and I/O-3 input typical application schematic

When I/O-2 and I/O-3 are configured as outputs, these can only be high-side switches and the output will be V_{SUP2} voltage. The R resistor shown on the I/O in Figure 44 is not required, but it is recommended to improve ESD performance and its value will be dependent on the circuitry the I/O has to drive.

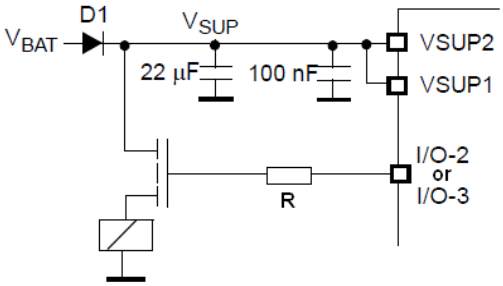


Figure 44. I/O-2 and I/O-3 output typical application schematic

The value of resistor R will also be determined by taking into account the maximum current capability of the I/O. Look at Table 6 for high-side capability of I/O-2 and I/O-3.

4.5.3 LIN-T1 and LIN-T2

LIN-T1 and LIN-T2 have dual functionality and can be configured as I/O-2 and I/O-3 correspondingly. These are disabled by default and must be configured by SPI during SBC initialization. They can be configured as LIN terminations for LIN master node applications or as I/O-2 or I/O3 depending on part number. When these are configured as LIN-Ts, they are controlled by the LIN register and will internally switch to V_{SUP2} as required by LIN master node application.

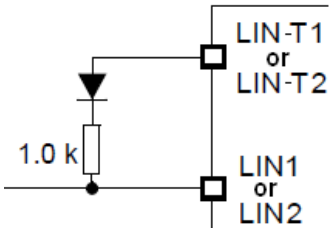


Figure 45. LIN-T1 and LIN-T2 typical application schematic

When LIN-T1 and LIN-T2 are configured to function as an I/O, these can be configured as wake-up inputs or high-side outputs. When configured as wake-up inputs, the SBC will wake-up on both a 'high' to 'low' or 'low' to 'high' transition. These can be configured to continuously monitor for transitions or 'cyclic sense wake-up' can be implemented on LIN-T1 and LIN-T2 to decrease module current consumption.

Table 7. LIN-T1 and LIN-T2 functionality

LIN	WU input	High-side	Low-side
T1	yes	20 mA	N/A
T2	yes	20 mA	N/A

A 22 kΩ resistor and a 100 nF decoupling capacitor are required for wake-up input implementation. R_{BAT} (10 kΩ recommended) is user defined depending on module current consumption requirements since it may potentially be connected to battery permanently (See Figure 46).

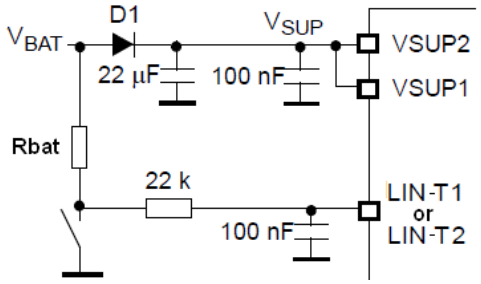


Figure 46. LIN-T1 and LIN-T2 input typical application schematic

When LIN-T1 and LIN-T2 are configured as outputs, these can only be high-side switches and the output will be V_{SUP2} voltage. The R2 resistor shown on the LIN-T in Figure 47 is not required, but it is recommended to improve ESD performance and its value will be dependent on the circuitry the I/O has to drive.

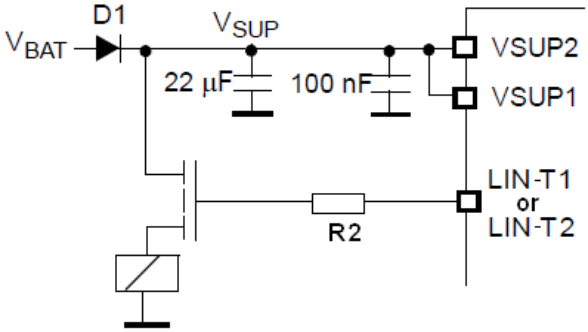


Figure 47. LIN-T1 and LIN-T2 output typical application schematic

The value of resistor R2 will also be determined by taking into account the maximum current capability of the LIN-T. Look at Table 7 for high-side capability for LIN-T1 and LIN-T2.

4.6 Safety interactions with microcontroller and debug

The MC33903/4/5 offers a wide range of functional safety features that allows the module designer to implement highly robust and reliable safety systems. The SBC's optional $\overline{\text{SAFE}}$ active low open drain output structure can be configured to trigger in case of a microcontroller failure, which could be indicated by multiple resets, RST pin shorted to GND, low V_{DD}, or missed watchdog/s. This will indicate that the module's microcontroller is no longer functional and a safety mechanism must be activated. $\overline{\text{SAFE}}$ pin must be left open if not used.

A safety implementation option is to activate a safety circuitry that is fully independent from the SBC or the microcontroller. Figure 48 shows this option and also allows the main MCU (microcontroller) to activate the safety circuitry even if the $\overline{\text{SAFE}}$ was not triggered. This adds system flexibility by allowing the MCU or the $\overline{\text{SAFE}}$ to activate the Safe Circuitry. All discrete components are determined by Safe Circuitry specifications.

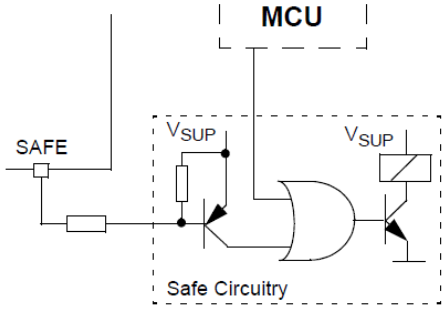


Figure 48. $\overline{\text{SAFE}}$ typical application schematic

Another option is to just turn ON an LED in case of a $\overline{\text{SAFE}}$ fault. Figure 49 show a simple way to accomplish this. The resistor is determined by the LED specifications.

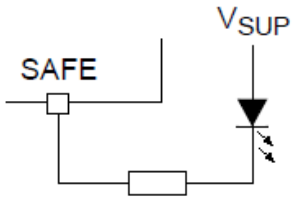


Figure 49. $\overline{\text{SAFE}}$ LED indicator typical application schematic

The MC33903/4/5 also implements a $\overline{\text{RST}}$ that allows for a system reset at first power up and for any other serious module conditions that may require a system reset such as battery faults generating VDD undervoltage conditions. The reset duration can be configured to 1.0 ms, 5.0 ms, 10.0 ms, or 20.0 ms via the SPI (1.0 ms by default) depending on application requirements. There are no additional discrete components required to connect the $\overline{\text{RST}}$ (internal ~11 kΩ pull-up to VDD) to the microcontroller, but a 10 kΩ pull-up resistor to VDD and a 100nF capacitor to GND are recommended for noise immunity and signal integrity on some applications.

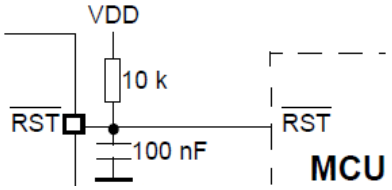


Figure 50. $\overline{\text{RST}}$ typical application schematic

The MC33903/4/5 also offers mask-able interrupts configurable to selectively trigger upon CAN and LIN faults, overvoltage and undervoltage conditions on VAUX, 5V-CAN, VSUP, and VSENSE, missed watchdog/s, thermal issues and overcurrent conditions. The $\overline{\text{INT}}$ duration can be configured to 25 us or 100 us (default) via the SPI depending on application requirements. Additionally, the microcontroller can request and $\overline{\text{INT}}$ as needed by sending a SPI command. There are no additional discrete components required to connect the $\overline{\text{INT}}$ (internal ~10 kΩ pull-up to VDD) to the microcontroller, but a 10 kΩ pull-up resistor to VDD is recommended for noise immunity and signal integrity on some applications.

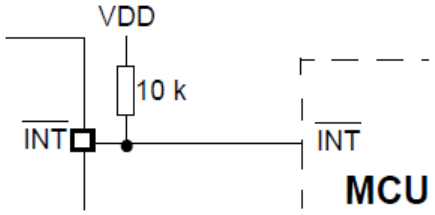


Figure 51. $\overline{\text{INT}}$ typical application schematic

The DBG (debug) pin has dual functionality. It can be used to run the SBC in debug mode (no need to monitor the watchdog) by placing 8.0 V - 10 V on pin or a resistor can be placed to GND. When the resistance to GND is implemented on this pin, the SBC will then react to a module fault in four different safe modes of the SBC depending on the DBG resistor value as shown in Figure 52.

			Resistor at DBG pin			
			MIN	TYP	MAX	SAFE MODE
	Description	Enable the SAFE RESITOR value check. If the SAFE resitor value is diferent of the range selected this will set a flag on SAFE register. INT generated to report this error. Additionaly in DEBUG mode or if a mismatch error between this config and the resistior range , this register will define the safe mode configuation and no consider the DBG resistance.				
SAFE_RES [2:0]	Default state	Disable				
	0xx	Disable (additionaly in DEBUG mode disable the SAFE mode detections)				
	100	After bus idle detection AND ignition signal low=> Turn Vdd OFF + WU enable	57.5k	68k		B3
	101	After ignition signal low=> Turn Vdd OFF + WU enable	27.5k	33k	34.5k	B2
	110	After bus idle detection=> Turn Vdd OFF + WU enable	14k	15k	16.5k	B1
	111	No further action			6k	A
	Reset condition	Power down (every time VSUV_BATFAIL is set)				

Figure 52. DBG resistor values for safe mode

One example circuit that can be implemented to run module in debug mode is by populating J27 and leaving J28 'open' in Figure 53, where the zener diode will maintain ~8.0 V on the DBG pin. The MC33903/4/5 also gives the flexibility to get out of debug mode by sending a specific SPI command (this overrides the hard-wired voltage on DBG).

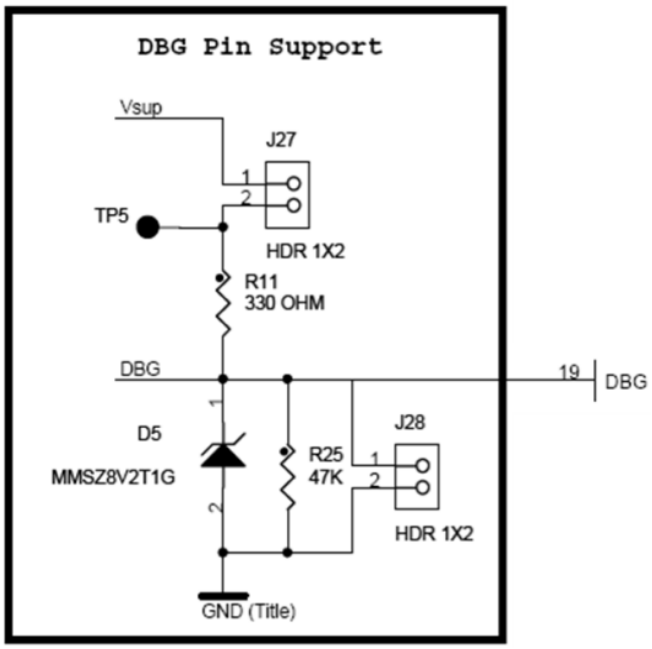


Figure 53. DBG typical application schematic

To run in typical mode (where watchdog has to be monitored), J27 should be left 'open' and J28 can be populated to allow SAFE MODE A functionality. To allow other SAFE MODE implementations, J27 and J28 can be left open and R25 can be interchanged to the corresponding SAFE MODE resistor value given in Figure 52.

4.7 CAN and LIN physical layers

The MC33903/4/5 implements one CAN physical layer and zero to two LIN physical layers dependent on part number (see Table 1, Table 2, and Table 3). The numerous variations of devices that combine both CAN and LIN communication protocols give the engineer great flexibility to design high conformance systems ranging from entry level modules to highly integrated high-end modules.

4.7.1 CAN

The CAN physical layer interface of the MC33903/4/5 is compliant to the ISO 11898-2 and ISO 11898-5 protocol specifications. This physical layer is specifically supplied by VSUP2 for all devices that have two supply inputs and VSUP for the rest of the devices, which only have a single supply input. The CAN physical layer is internally supplied by the 5V-CAN regulator and communicates with the microcontroller via TxD and RxD. CANH and CANL are biased to 2.5 V when the bus is in recessive state and to GND when the transceiver is in sleep state.

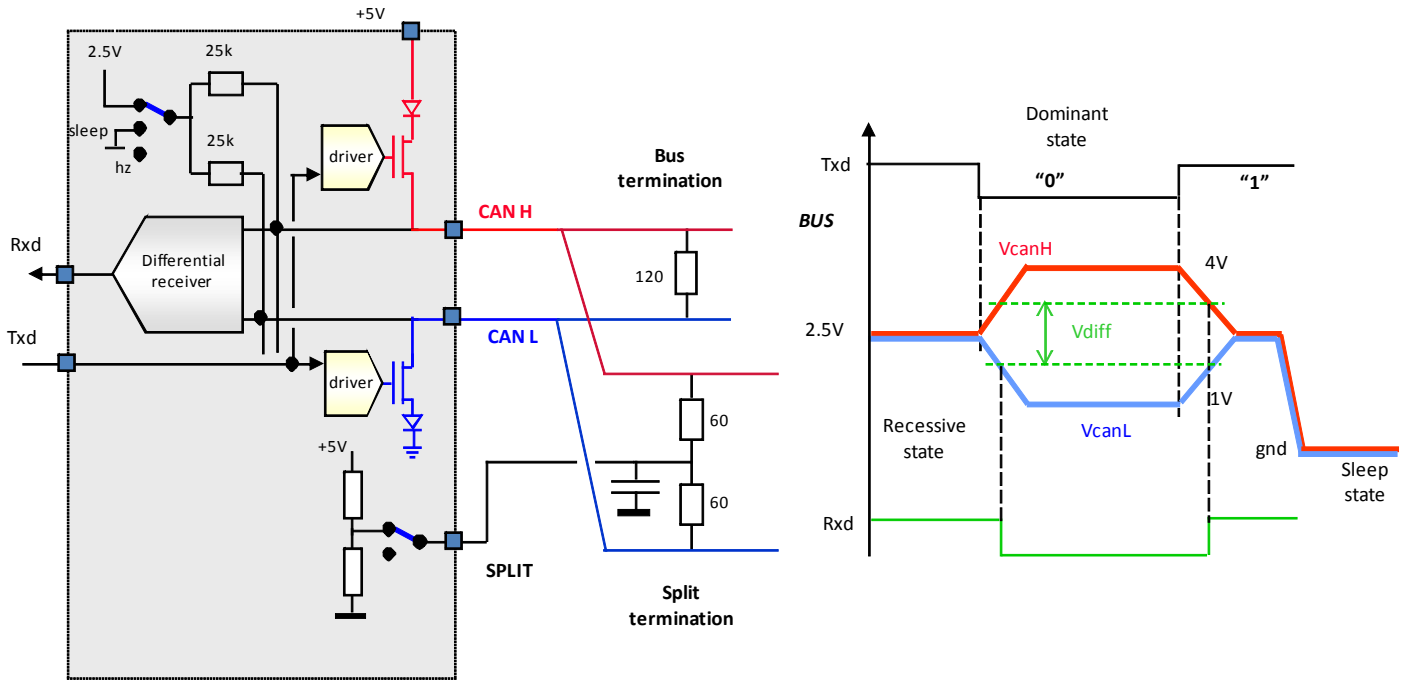
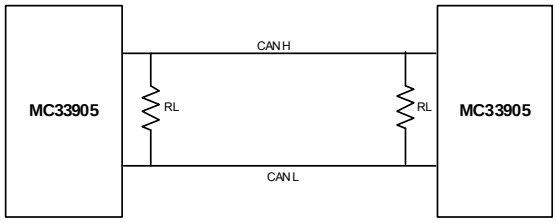


Figure 54. High speed CAN physical interface

The general CAN network architecture is driven by the ISO 11898 specification and requires that two nodes be terminated with 120 Ω resistors on both ends of the twisted pair network. As shown in Figure 55.



Notation	Unit	Value			Condition
		min.	nom.	max.	
RL[a)]	O	100	120	130	Min. power dissipation: 220 mW.

a) Dependent on the topology, the Bit rate, and the slew rate deviations from 120 O may be possible. It is, however, necessary to check the applicability of other resistor values in each case. It is furthermore possible to use a single central bus termination. In this case the termination concentrates into one resistor with the value RL / 2 offering a power dissipation of at least 440 mW. This central termination might also be implemented using a split termination consisting out of 2 resistors with each RL / 4 and at least 220 mW per resistor.
The power dissipation is calculated based on the maximum differential bus voltage of 5V, which is independent from the battery supply system. In case short circuits on the bus wires towards battery have to be supported, the minimum required power dissipation increases depending on the assumed maximum short circuit bus voltage.
Remark : The lower the termination resistor value is the smaller the number of nodes in a network is due to the internal differential resistors of all receivers connected to the bus lines CAN_H and CAN_L.

Figure 55. High speed CAN network architecture

The non-terminated nodes should be connected to the network as shown on Figure 56 to comply with the CAN bus network topology as specified by the ISO 11898.

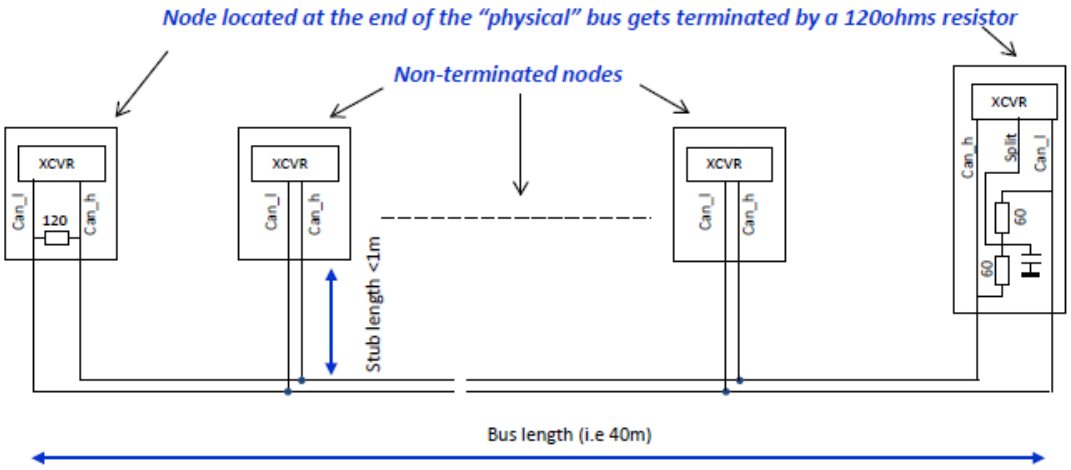


Figure 56. High speed CAN network topology

The MC33903/4/5 implements a highly robust CAN interface which can sustain ESD pulses up to +/-8 kV (Human Body Model) at the CANH and CANL pins. If application requires higher ESD voltage robustness, external protection components such as a transient voltage suppressor (TVS) are required to protect these pins. The MMB27VCLT1 (D) is recommended to achieve better ESD results (see Figure 57). Implementing this TVS will improve ESD performance up to +/-15 kV according to ISO 10605-2008 (ESD powered). Additionally, a 47 pF capacitor (C) should be placed on the CANH and CANL pins for noise immunity, ESD, and to lower noise emissions. Figure 58 shows the recommended circuitry for the CAN transceiver.

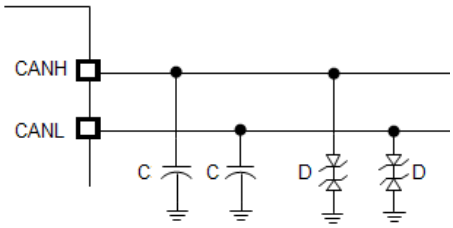


Figure 57. CANH and CANL ESD external protection typical application schematic

Optionally, a common mode choke (L1) may be implemented on the CAN transceiver if the application requires it. If this is the case, the TDK ACT45B-510 is recommended for noise immunity and emissions. This will increase the immunity for RF noise and lower the noise emitted by the CAN transceiver. Note that the MC33903/4/5 has been EMC certified according to SAE J2962-2 without the need to include a common mode choke on the CAN physical layer.

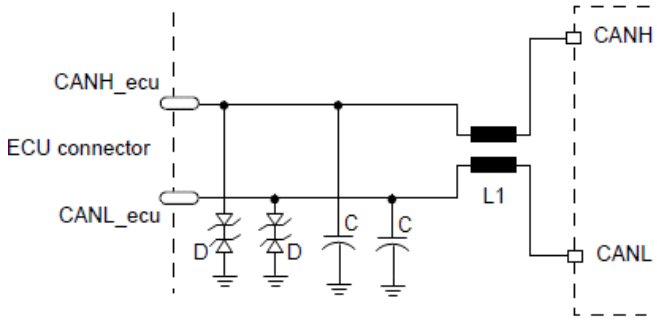


Figure 58. CANH and CANL typical application schematic

The MC33903/4/5 offers a SPLIT pin that can optionally be implemented to further improve EMC performance and signal stability during recessive state of the CAN bus. This also adds flexibility and various options for connecting the terminating CAN nodes. If SPLIT is not used, it must be left open.

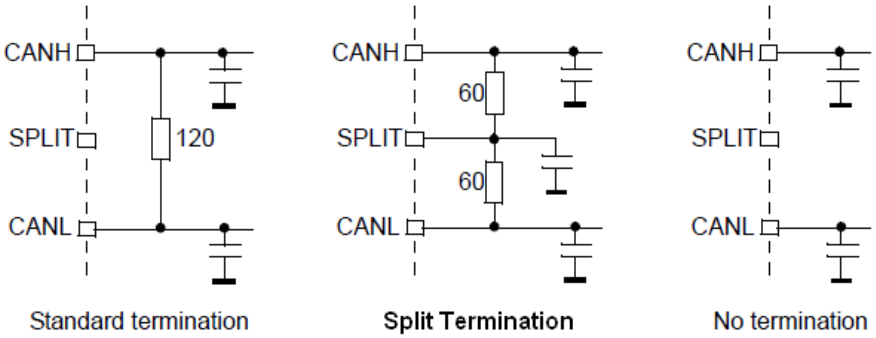


Figure 59. CAN termination options

4.7.2 LIN

The MC33903/4/5 offers zero to two LIN transceivers that are compliant to LIN 2.1 and J2602-2 protocol specifications. The LIN interfaces are specifically supplied by VSUP2 for all devices that have two supply inputs and Vsup for the rest of the devices, which only have a single supply input. Similar to the CAN transceiver, the LIN interface communicates with the microcontroller via TxD and RxD, but at slower baud rates and under a different communication protocol.

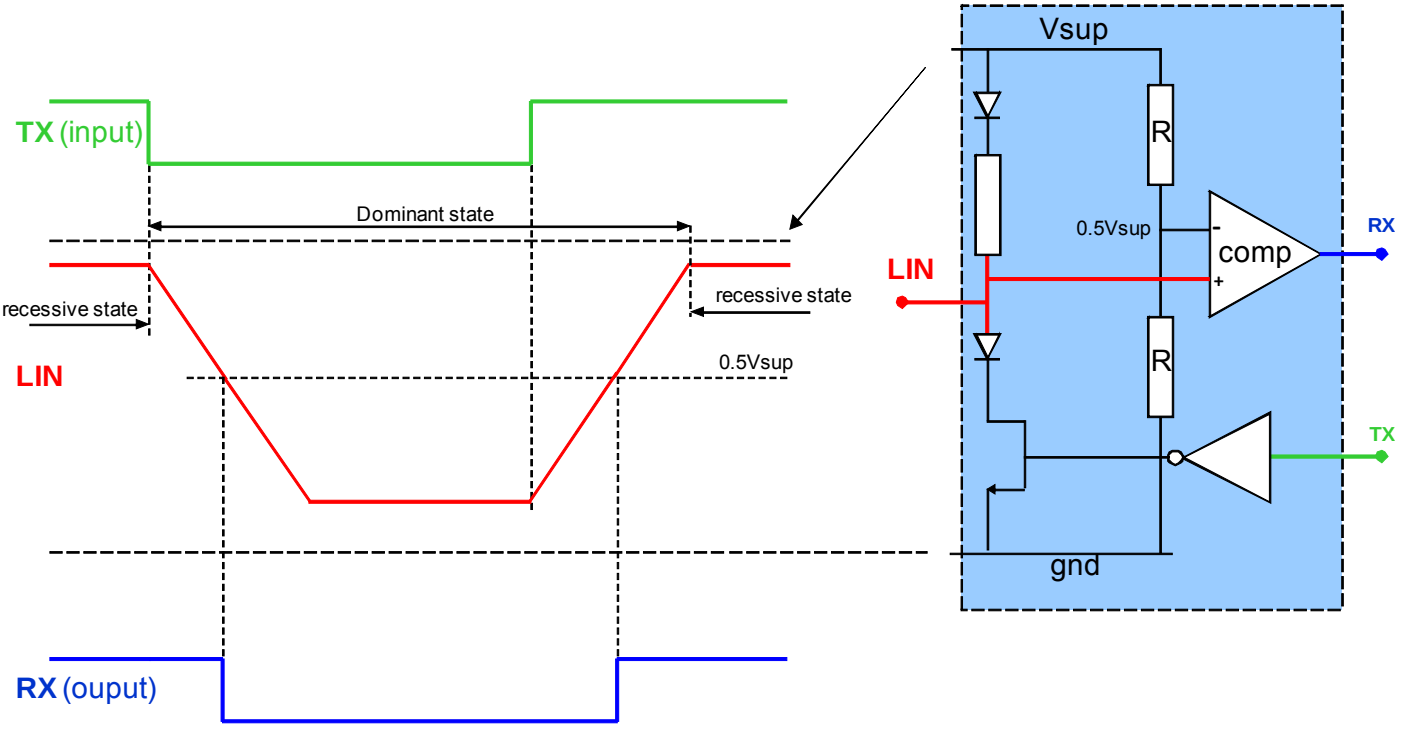


Figure 60. LIN physical interface

The bus topology is based on single master and multiple slave architecture (see Figure 61). The master module must implement an external 1.0 kΩ pull-up resistor to VSUP in series with a diode. This is to prevent current flowing from the LIN bus into the module and creating an uncontrolled power supply in case of a 'loss of battery'.

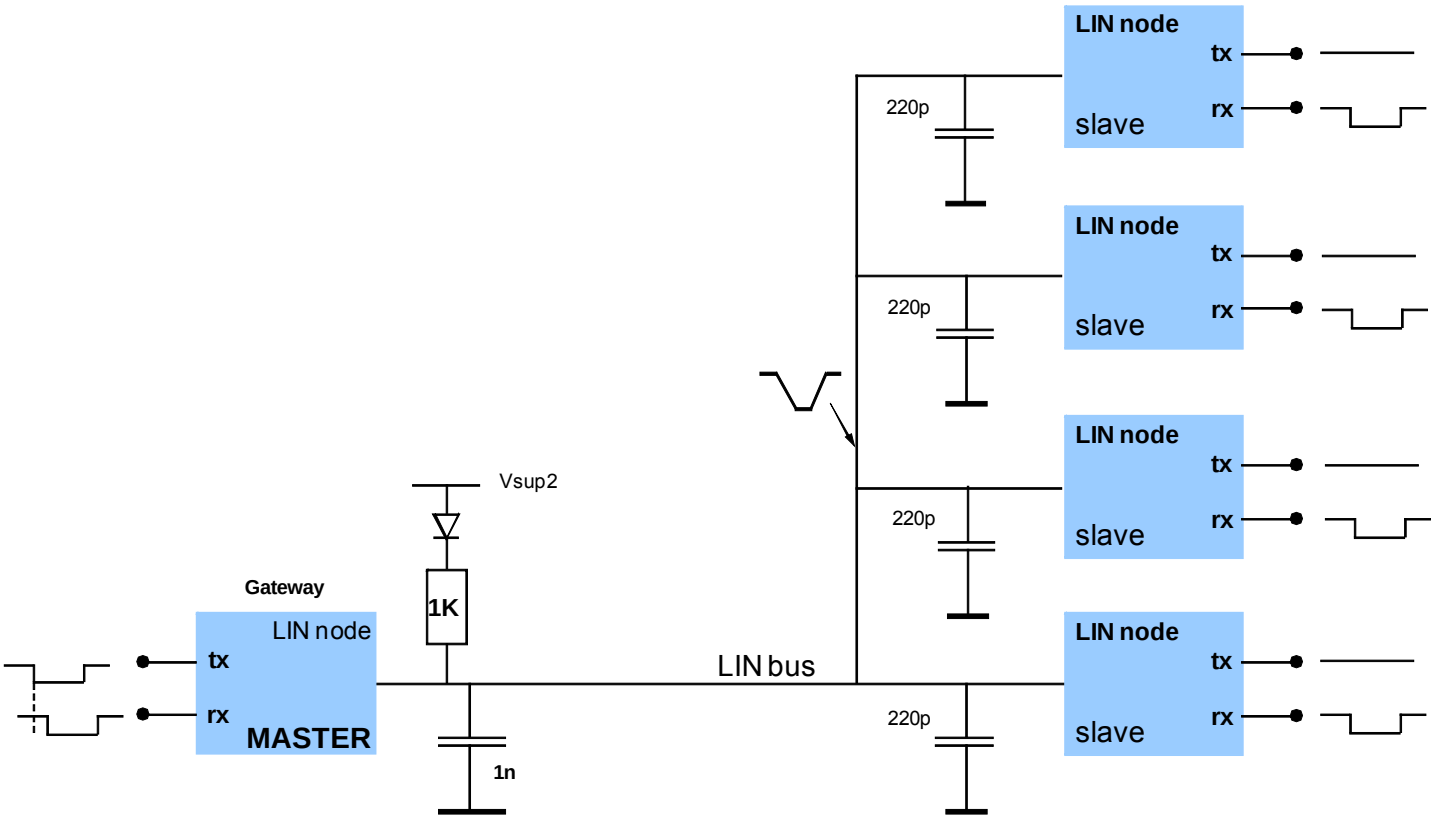


Figure 61. LIN network topology

There are two circuitry options for master LIN nodes. The SBC's LIN-Termination pin can be implemented or the 1.0 kΩ resistor and diode can be connected directly to VSUP (see Figure 62). The recommended diode is 1N4148WS and the resistor can be +/-10% accurate. For better EMC performance, a capacitor must be placed on the LIN pin. The value of this capacitor is subject to OEM approval, it is recommended to have a minimum of 68 pF.

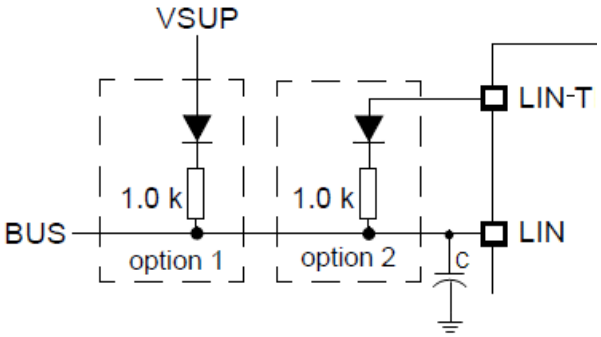


Figure 62. LIN master node application schematic options

5 Programming the SBC

Once the module circuitry is all laid out, the designer can then start the software development. The MC33903/4/5 requires some simple, but important initialization and feature configurations that will allow maximizing the functional safety aspects of the SBC. Because the feature set is different dependent on part number, the software may differ from application to application. Note that if the software has been written to drive the MC33905D and exercise all of its features and safety aspects, this same software can be used to drive ANY of the MC33903/4/5 SBCs. The commands that are sent, for which the specific SBC does not have the feature, will be ignored and will not have a negative effect on the module's functionality.

5.1 SPI

The communication between the SBC and the module's microcontroller is driven by type 2 Serial Peripheral Interface (SPI), where the data is changed on the rising edge of SCLK and sampled on the falling edge as shown on Figure 63.

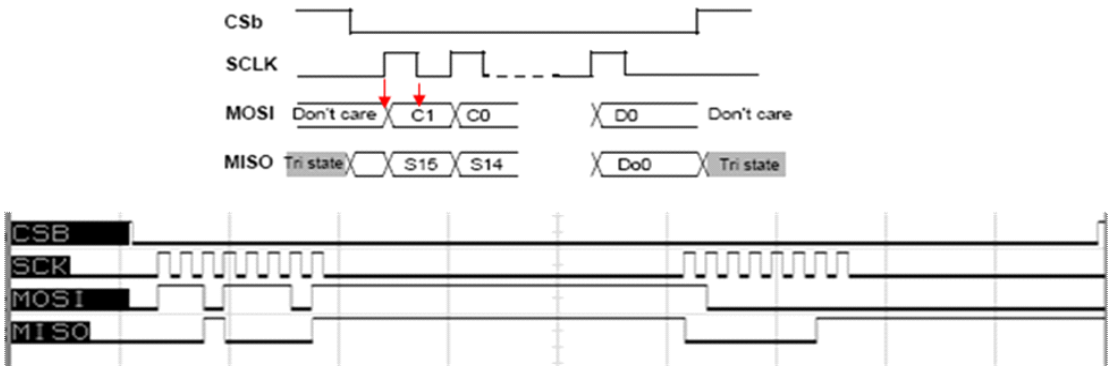


Figure 63. Serial peripheral interface

Note: SPI does not have daisy chain capability.

Via SPI, the microcontroller can write to specific registers, read these registers to verify content and device status, and additionally it can read any device status flags that may have been set.

The maximum operating frequency for the SPI bus is 4.0 MHz and it's made up of 16 bits (except for 1 watchdog refresh case). It implements optional parity and any SPI message sent that is not a multiple of 8 clock pulses will be ignored and generate an interrupt. The SPI bus also has $\overline{CS}$ short to GND detection. Any SPI message sent will return valid device status data on MISO (i.e. CAN failure, I/O failure, Wake-up, etc.) There are 32 SPI bit register addresses and the overall SPI architecture is as shown on Figure 64.

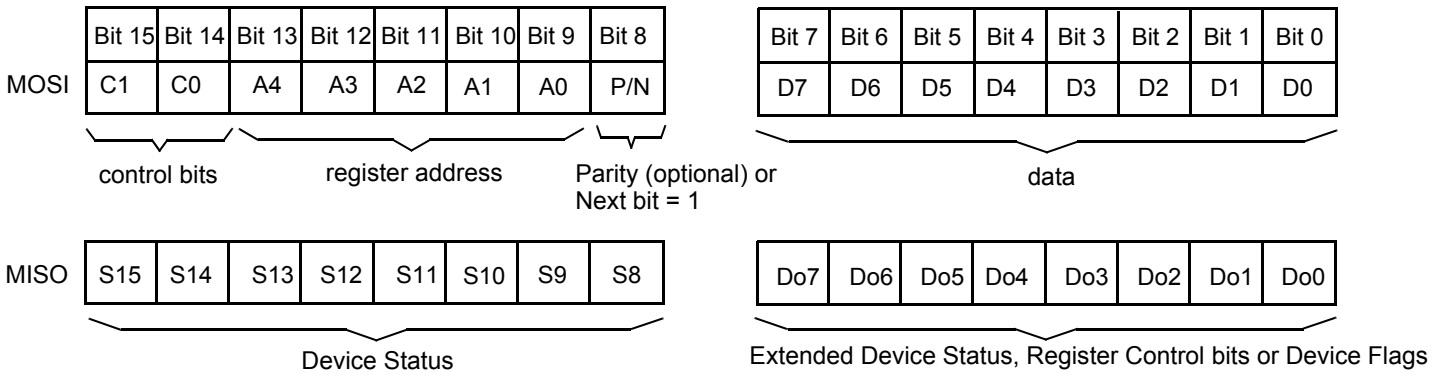


Figure 64. SPI read and write functionality

Bits 15 and 14 are the control bits to determine if the SPI word sent is a write to register address, read back of the register address, or a read of the device's flags from a register address. Bit 8 is for optional parity selection where a 0 represents no parity and a 1 represents parity is selected. Refer to the datasheet for more parity details.

Table 8. SPI operations (bits 8, 14, & 15)

Control bits MOSI[15-14], C1-C0	Type of command	Parity/next MOSI[8] P/N	Note for bit 8 P/N
00	Read back of register content and block (CAN, I/O, INT, LINs) real time state. See Table 12.	1	Bit 8 must be set to 1, independently of the parity function selected or not selected.
01	Write to register address, to control the device operation	0	If bit 8 is set to “0”: means parity not selected OR parity is selected AND parity = 0
		1	if bit 8 is set to “1”: means parity is selected AND parity = 1
10	Reserved		
11	Read of device flags form a register address	1	Bit 8 must be set to 1, independently of the parity function selected or not selected.

Bits 13 - 9 are the register address bits and are mapped in Table 9.

Table 9. Device registers with corresponding address

Address MOSI[13-9] A4...A0	Description	Quick Ref. Name	Functionality
0_0000	Analog Multiplexer	MUX	1) Write “device control bits” to register address. 2) Read back register “control bits”
0_0001	Memory byte A	RAM_A	1) Write “data byte” to register address. 2) Read back “data byte” from register address
0_0010	Memory byte B	RAM_B	
0_0011	Memory byte C	RAM_C	
0_0100	Memory byte D	RAM_D	
0_0101	Initialization Regulators	Init REG	1) Write “device initialization control bits” to register address. 2) Read back “initialization control bits” from register address
0_0110	Initialization Watchdog	Init watchdog	
0_0111	Initialization LIN and I/O	Init LIN I/O	
0_1000	Initialization Miscellaneous functions	Init MISC	
0_1001	Specific modes	SPE_MODE	1) Write to register to select device Specific mode, using “Inverted Random Code”. 2) Read “Random Code”
0_1010	Timer_A: watchdog & LP MCU consumption	TIM_A	1) Write “timing values” to register address. 2) Read back register “timing values”
0_1011	Timer_B: Cyclic Sense & Cyclic Interrupt	TIM_B	
0_1100	Timer_C: watchdog LP & Forced Wake-up	TIM_C	
0_1101	Watchdog Refresh	watchdog	Watchdog Refresh Commands
0_1110	Mode register	MODE	1) Write to register to select LP mode, with optional “Inverted Random code” and select Wake-up functionality 2) Read operations: Read back device “Current mode” Read “Random Code”, Leave “Debug mode”

Table 9. Device registers with corresponding address (continued)

Address MOSI[13-9] A4...A0	Description	Quick Ref. Name	Functionality
0_1111	Regulator Control	REG	1) Write “device control bits” to register address, to select device operation. 2) Read back register “control bits”. 3) Read device flags from each of the register addresses.
1_0000	CAN interface control	CAN	
1_0001	Input Output control	I/O	
1_0010	Interrupt Control	Interrupt	
1_0011	LIN1 interface control	LIN1	
1_0100	LIN2 interface control	LIN2	

5.2 SBC Modes

The MC33903/4/5 family of SBCs has various modes of operation to accommodate the majority of module requirements such as low current consumption with microcontroller completely OFF or ON with limited functionality capability, flashing of the module, microcontroller soft start, etc. The SBC has eight different states it can transition through after power up as shown in Figure 65.

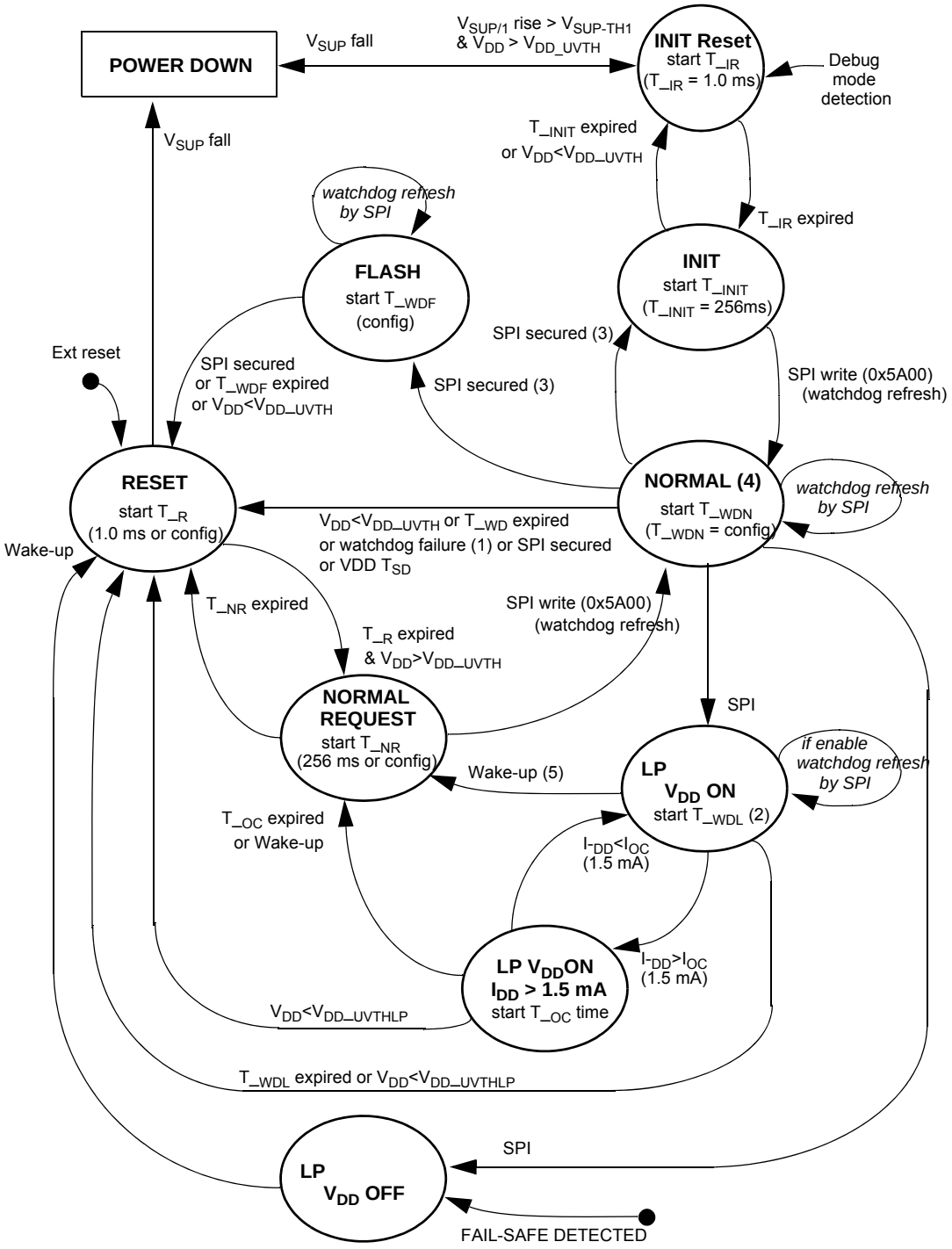


Figure 65. State diagram

5.2.1 Debug mode

Debug mode is a special operation implementation of the MC33903/4/5 family of SBCs that allows for easy debugging of the software and hardware. When debug mode is detected, all software watchdog operations are disabled. The 256 ms in INIT mode, watchdog refresh of Normal and Flash modes, Normal Request time out (256 ms or user defined) are disabled and do not lead into an INIT Reset or Reset mode transition. When the SBC is running in debug mode, a SPI command can be sent without any watchdog operation time constraints. The MCU software can be debugged in real-time and halted when necessary to verify proper operation.

Note: SAFE mode functionality is also available in debug mode operation. In this case, the SBC will activate SAFE mode B2 as shown in Figure 70 (regardless of the resistor value on the DBG pin).

To set the device in Debug mode, 8.0 V to 10 V must be applied on the DBG pin before powering up the SBC. When the SBC transitions from INIT Reset into INIT mode, it will detect if the voltage at the DBG pin is within the specified 8.0 V - 10.0 V range.

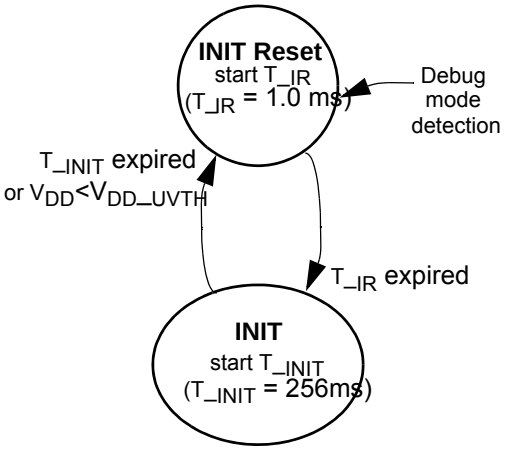


Figure 66. Init reset and INIT state diagram

If debug voltage condition is met, the SBC will activate the debug mode operation. The debug status of the device is reported via a flag in the Device Modes register (0xDD80). See Table 10 for more details.

Table 10. Device Modes

Global commands and effects								
Read device current mode, Leave debug mode. Keep SAFE pin as is. MOSI in hexadecimal: 1D 00	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		00	01 110	1	0	000 0000		
	MISO	**bit 15-8**		bit 7-3		bit 2-0		
		Fix Status		device current mode		Random code		
Read device current mode Release SAFE pin (turn OFF). MOSI in hexadecimal: 1D 80	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		00	01 110	1	1	000 0000		
	MISO	**bit 15-8**		bit 7-3		bit 2-0		
		Fix Status		device current mode		Random code		
Read device current mode, Leave debug mode. Keep SAFE pin as is. MOSI in hexadecimal: DD 00 MISO reports Debug and SAFE state (bits 1,0)	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		11	01 110	1	0	000 0000		
	MISO	**bit 15-8**		bit 7-3		bit 2	bit 1	bit 0
		Fix Status		device current mode		X	SAFE	DEBUG

Table 10. Device Modes (continued)

Global commands and effects								
Read device current mode, Keep DEBUG mode Release SAFE pin (turn OFF). MOSI in hexadecimal: DD 80 MISO reports Debug and SAFE state (bits 1,0)	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		11	01 110	1	1	000 0000		
	MISO	**bit 15-8**		bit 7-3		bit 2	bit 1	bit 0
		Fix Status		device current mode		X	SAFE	DEBUG

If the voltage on the DBG pin falls below the specified 8V, the SBC will exit debug mode, all the watchdog operations are enabled, and a proper watchdog refresh is expected. The SBC can also exit out of debug mode by reading the Device Modes register (0xDD00) as specified in Table 10. This SPI command has priority over the voltage measured on the DBG pin and is especially useful when the module requires exiting out of debug mode regardless of the hardware configuration.

5.2.2 SAFE Modes

The MC33903/4/5 family of SBC includes four different SAFE modes that are hardware configuration selectable by means of a specific resistor value placed on the DBG pin (see Table 11). These SAFE Modes can also be verified and initialized by software SPI command. The INIT MISC register allows for the SAFE mode verification and modification (see Table 16). This functional safety feature provides flexibility to the module designer to implement a robust and safe system. The fast reaction of the SBC to a module fault is predictable and can accommodate for lower power consumption in such event. The SAFE output also provides a 'plan B' in case of a microcontroller failure where the module will be placed in a known state.

Note: SAFE mode functionality is also available in debug mode operation. In this case, the SBC will activate SAFE mode B2 as shown in Figure 70 (regardless of the resistor value on the DBG pin).

Table 11. Fail-safe Options

Resistor at DBG pin	SPI coding - register INIT MISC bits [2,1,0] (higher priority that resistor coding)	Safe mode code	V_{DD} status
<6.0 k	bits [2,1,0) = [111]: verification enable: resistor at DBG pin is typically 0 kΩ (RA) - Selection of SAFE mode A	A	remains ON
typically 15 k	bits [2,1,0) = [110]: verification enable: resistor at DBG pin is typically 15 kΩ (RB1) - Selection of SAFE mode B1	B1	Turn OFF 8.0 s after CAN traffic bus idle detection.
typically 33 k	bits [2,1,0) = [101]: verification enable: resistor at DBG pin is typically 33 kΩ (RB2 - Selection of SAFE mode B2	B2	Turn OFF when I/O-1 low level detected.
typically 68 k	bits [2,1,0) = [100]: verification enable: resistor at DBG pin is typically 68 kΩ (RB3) - Selection of SAFE mode B3	B3	Turn OFF 8.0 s after CAN traffic bus idle detection AND when I/O-1 low level detected.

The SAFE active 'low' output is triggered upon a watchdog failure, multiple resets, VDD low, or if the RST pin is shorted to GND. The SBC reaction to any of these faults will then be dependent on the resistor value on the DBG pin. The V_{DD} may remain ON or turn OFF after specified conditions are met (see Table 11).

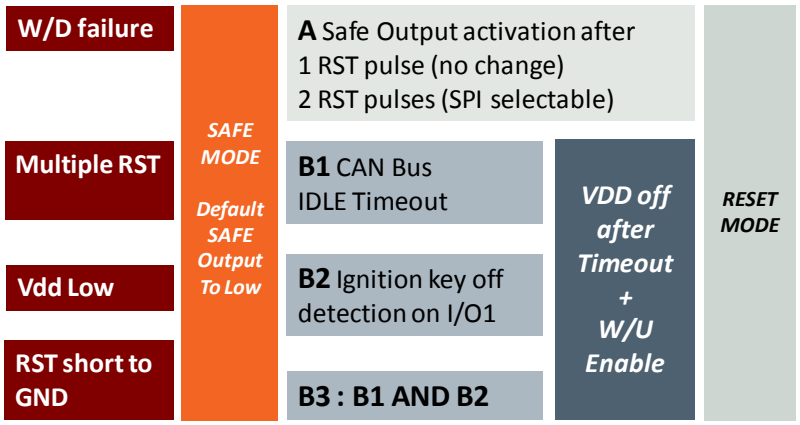


Figure 67. Fail-safe modes

When the SBC goes into SAFE mode A, the VDD remains ON keeping the microcontroller powered up until the failure condition recovers and the microcontroller is then able to properly control the device and refresh the watchdog. The SAFE output activation can be initialized to trigger on the first missing watchdog or on the second consecutive missing watchdog (refer to Figure 68) via the INIT Watchdog register specified in Table 14.

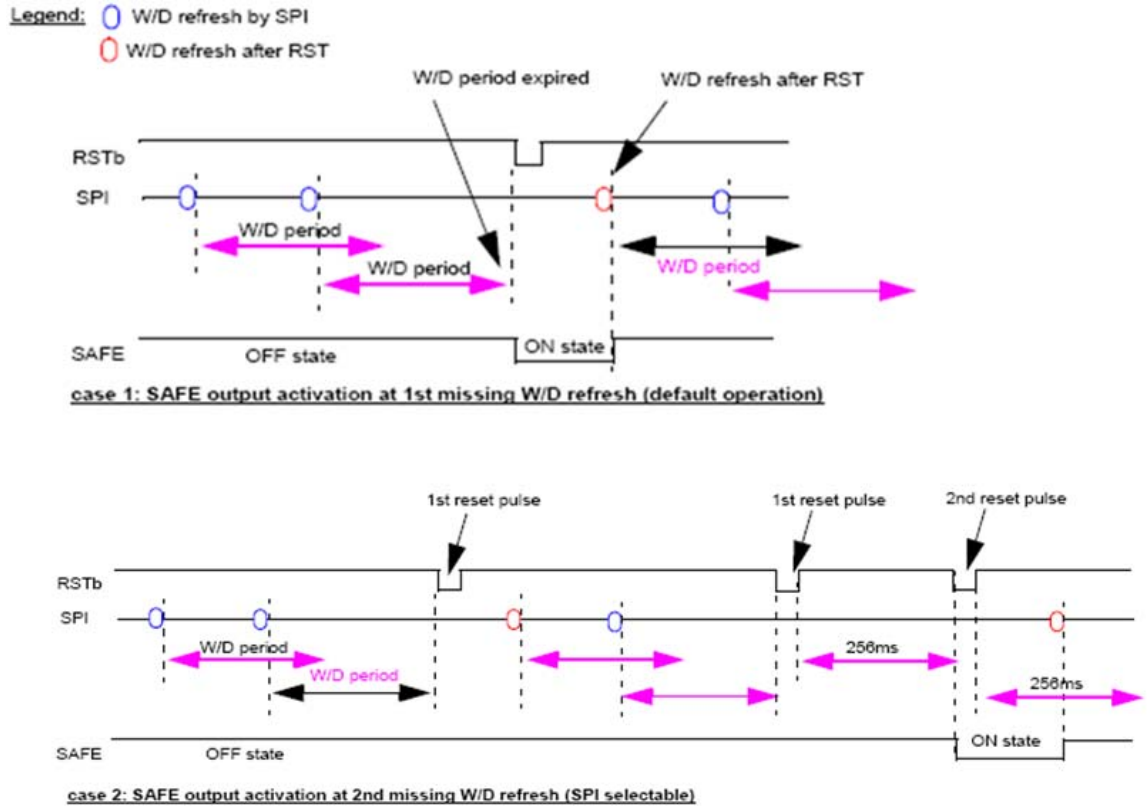


Figure 68. Watchdog and fail-safe operation

During SAFE mode B1, the VDD will remain ON keeping the microcontroller powered up for as long as the CAN bus is active. The VDD will shut down if CAN bus traffic goes idle for typically 8.0 seconds, but the SBC is CAN and I/O-1 wake-up enabled allowing the system to recover.

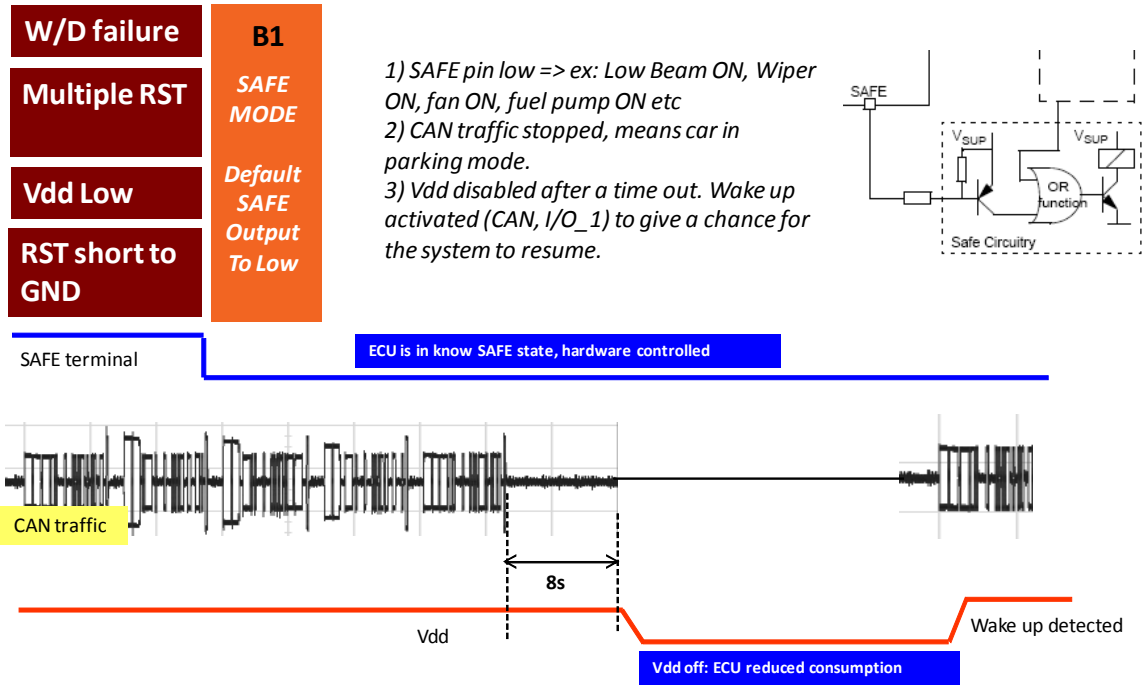


Figure 69. SAFE mode B1

During SAFE mode B2, the VDD will remain ON keeping the microcontroller powered up until an I/O-1 'low' level is detected, but the SBC is CAN and I/O-1 wake-up enabled allowing the system to recover.

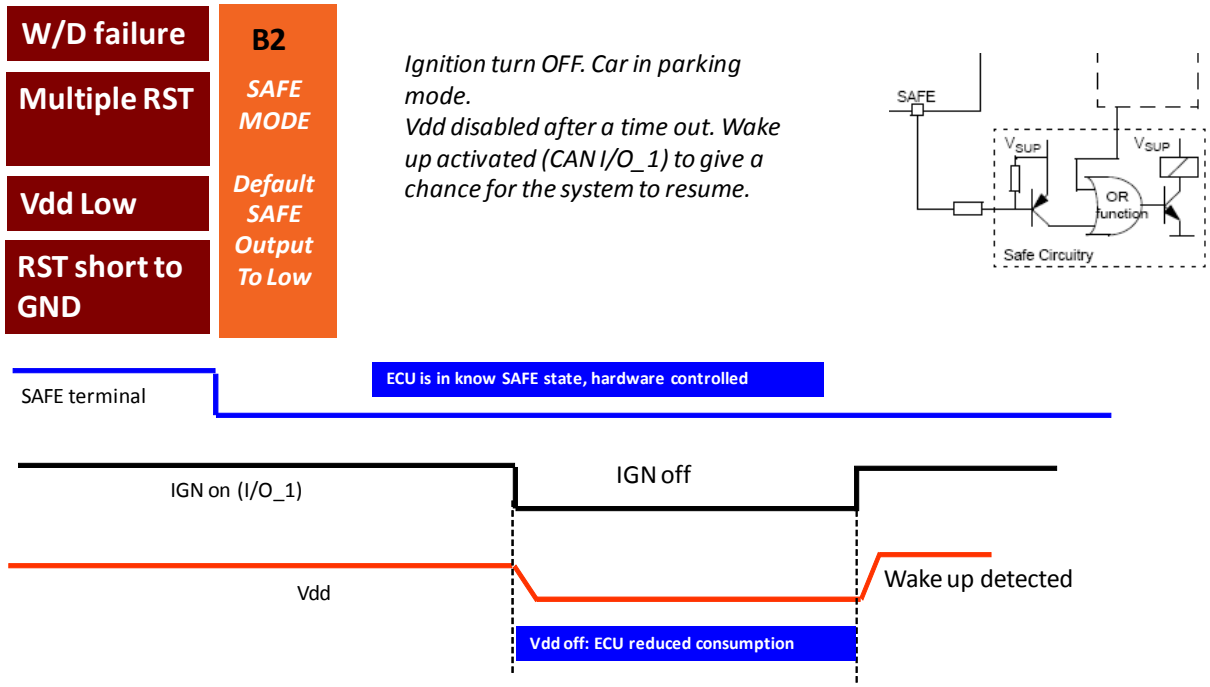


Figure 70. SAFE mode B2

SAFE mode B3 combines SAFE modes B1 and B2. During SAFE mode B3, the VDD will remain ON keeping the microcontroller powered up until the CAN bus goes idle for typically 8 seconds AND an I/O-1 'low' level is detected, but the SBC is CAN and I/O-1 wake-up enabled allowing the system to recover.

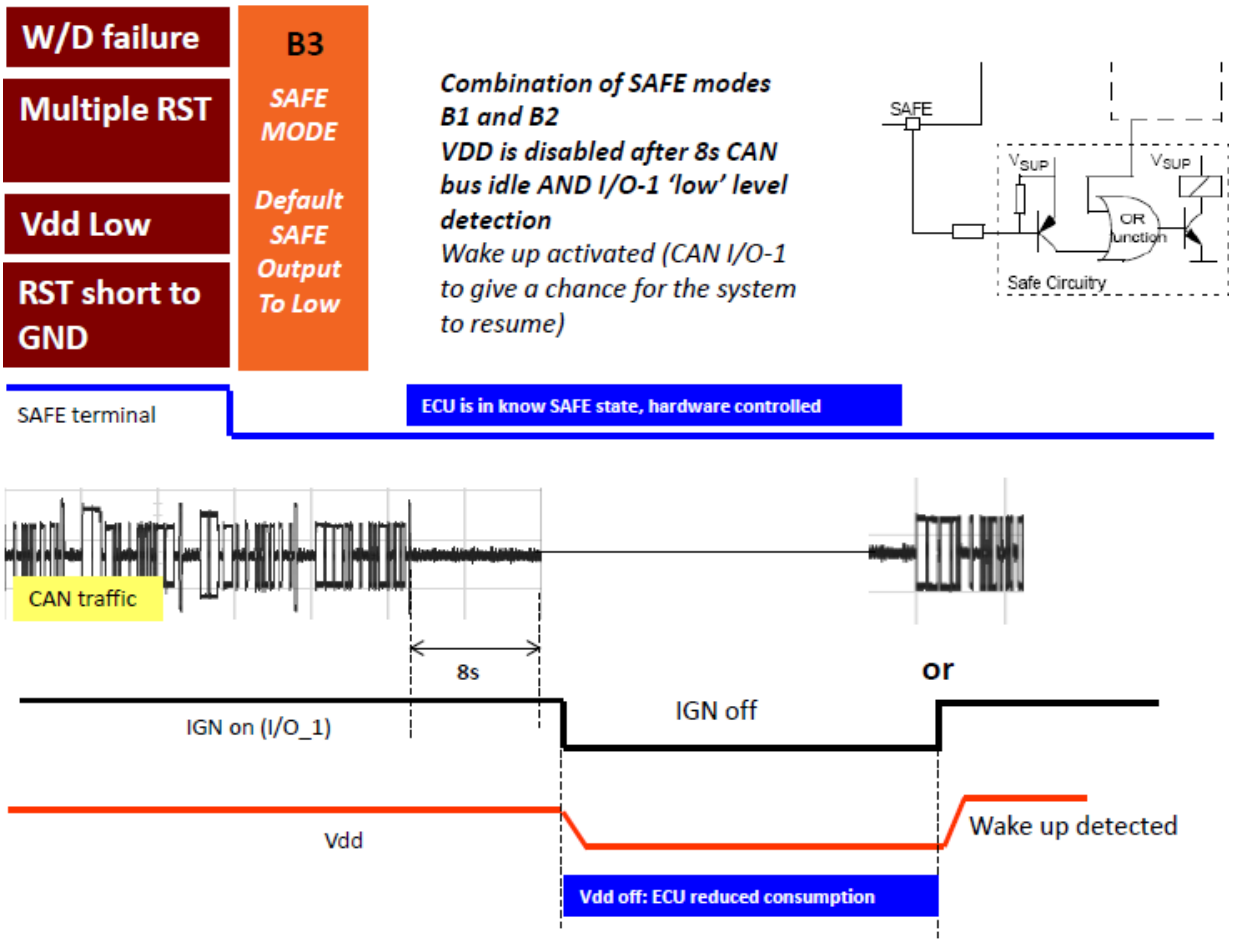


Figure 71. SAFE mode B3

5.3 Flags and device status

It is very important to read the SBC's flags and acquire the real time status of the SBC's feature set after power up and after any mode transition or wake-up. This information will enable the microcontroller to react accordingly dependent on module's requirements. It is also recommended to periodically read the flags that may have been set and the SBC feature set status as required by application. This allows for the design of a highly flexible, smart, and functional safe system due to enhanced diagnostics where wake-up, interrupts, and reset sources and faults can be identified. Refer to Table 12 and the datasheet for further flag description details.

Table 12. Device flag, I/O real time and device identification

Bits	15-14	13-9	8	7	6	5	4	3	2	1	0
MOSI	MOSI bits 15-7			Next 7 MOSI bits (bits 6.0) should be “000_0000”							
	bits [15, 14]	Address [13-9]	bit 8	bit 7							
MISO	8 Bits Device Fixed Status (bits 15...8)			MISO bits [7-0], device response on MISO pin							
				bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Table 12. Device flag, I/O real time and device identification (continued)

Bits	15-14	13-9	8	7		6	5	4	3	2	1	0
REG	11	0_1111 REG	1	0	V_{AUX_LOW}	$V_{AUX\_OVERCURRENT}$	$5V_{-CAN\_}$ THERMAL SHUTDOWN	$5V_{-CAN\_}$ UV	$5V_{-CAN\_}$ OVERCURRENT	$V_{SENSE\_}$ LOW	$V_{SUP\_}$ UNDERVOLTAGE	$I_{DD\text{-}OC\text{-}NORMAL\ MODE}$
	11			1	-	-	-	$V_{DD\_}$ THERMAL SHUTDOWN		R_{ST_LOW} (<100 ms)	$V_{SUP\_}$ BATFAIL	$I_{DD\text{-}OC\text{-}LP}$ V_{DD} ON MODE
	Hexa SPI commands to get Vreg Flags: MOSI 0x DF 00, and MOSI Ox DF 80											
CAN	11	1_0000 CAN	1	0	CAN Wake-up	-	CAN Overtemp	RXD low	Rxd high	TXD dom	Bus Dom clamp	CAN Overcurrent
				1	CAN_UF	CAN_F	CANL to V_{BAT}	CANL to V_{DD}	CANL to GND	CANH to V_{BAT}	CANH to V_{DD}	CANH to GND
	Hexa SPI commands to get CAN Flags: MOSI 0x E1 00, and MOSI 0x E1 80											
	00	1_0000 CAN	1	1	CAN Driver State	CAN Receiver State	CAN WU en/dis	-	-	-	-	-
	Hexa SPI commands to get CAN real time status: MOSI 0x 21 80											
I/O	11	1_0001 I/O	1	0	HS3 short to GND	HS2 short to GND	SPI parity error	$\overline{CS}$ low >2.0 ms	$V_{SUP/2\text{-}UV}$	$V_{SUP/1\text{-}OV}$	I/O_O thermal	watchdog flash mode 50%
				1	I/O_1-3 Wake-up	I/O_0-2 Wake-up	SPI Wake-up	FWU	INT service Timeout	LP V_{DD} OFF	Reset request	Hardware Leave Debug
	Hexa SPI commands to get I/O Flags and I/O Wake-up: MOSI 0x E3 00, and MOSI 0x E3 80											
	00	1_0001 I/O	1	1		I/O_3 state		I/O_2 state		I/O_1 state		I/O_0 state
	Hexa SPI commands to get I/O real time level: MOSI 0x 23 80											
SAFE	11	1_0010 SAFE	1	0	INT request	RST high	DBG resistor	V_{DD} temp Pre-warning	V_{DD} UV	V_{DD} Overvoltage	$V_{AUX\_overVOLTAGE}$	-
				1	-	-	-	V_{DD} low >100 ms	V_{DD} low RST	RST low >100 ms	multiple Resets	watchdog refresh failure
	Hexa SPI commands to get INT and RST Flags: MOSI 0x E5 00, and MOSI 0x E5 80											
	00	1_0010 SAFE	1	1	V_{DD} (5.0 V or 3.3 V)	device p/n 1	device p/n 0	id4	id3	id2	id1	id0
	Hexa SPI commands to get device Identification: MOSI 0x 2580 example: MISO bit [7-0] = 1011 0100: MC33904, 5.0 V version, silicon Rev. C (Pass 3.3)											
LIN/1	11	1_0011 LIN 1	1	0	-	LIN1 Wake-up	LIN1 Term short to GND	LIN 1 Overtemp	RXD1 low	RXD1 high	TXD1 dom	LIN1 bus dom clamp
	Hexa SPI commands to get LIN 2 Flags: MOSI 0x E7 00											
	00	1_0011 LIN 1	1	1	LIN1 State	LIN1 WU en/dis	-	-	-	-	-	-
	Hexa SPI commands to get LIN1 real time status: MOSI 0x 27 80											
LIN2	11	1_0100 LIN 2	1	0	-	LIN2 Wake-up	LIN2 Term short to GND	LIN 2 Overtemp	RXD2 low	RXD2 high	TXD2 dom	LIN2 bus dom clamp
	Hexa SPI commands to get LIN 2 Flags: MOSI 0x E9 00											

Table 12. Device flag, I/O real time and device identification (continued)

Bits	15-14	13-9	8	7		6	5	4	3	2	1	0
	00	1_0100 LIN 2	1	1	LIN2 State	LIN2 WU en/dis	-	-	-	-	-	-
	Hexa SPI commands to get LIN2 real time status: MOSI 0x 29 80											

5.4 Initializing the SBC

After powering up the SBC, it will transition into the INIT Reset state when the V_{SUP} voltage goes above the $V_{SUP\text{-}TH1}$ threshold (typ. 4.1 V) and V_{DD} goes above the V_{DD_UVTH} (typ. 4.6 V). As the $V_{SUP/1}$ voltage ramps up, the slope controlled V_{DD} will follow and the RST pin stays asserted 'low' as shown in Figure 72. Once V_{DD} reaches the V_{DD_UVTH}, the INIT mode counter starts counting up to 1.0 ms (default) based on the internal oscillator, which is powered by VSUP1. Within this 1.0 ms time frame, 5V_CAN starts and DBG pin is checked for debug mode. After the 1.0 ms time frame, the SBC enters into INIT state and $\overline{RST}$ is released.

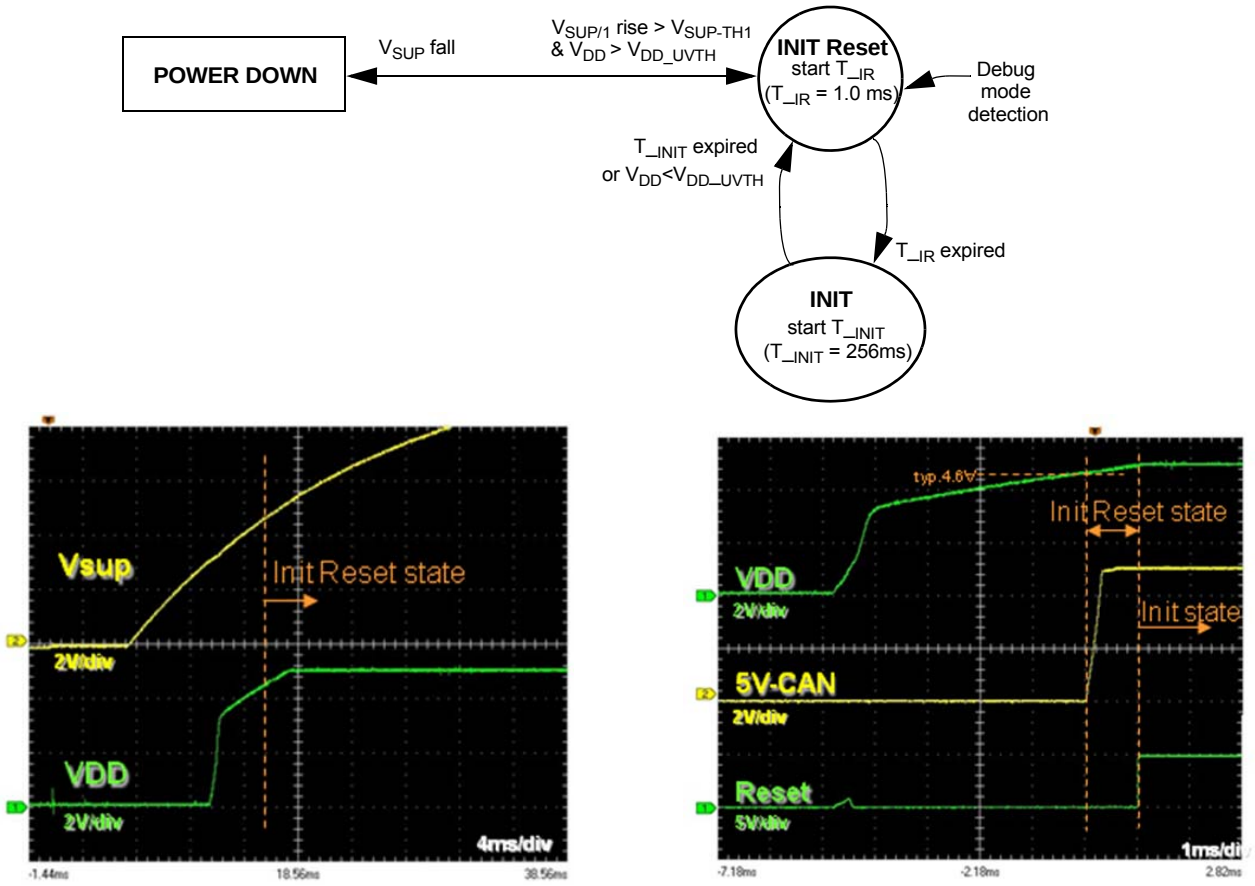


Figure 72. Initialization after power-up

Once the SBC enters into the INIT state, the T_init mode counter starts counting up to 256 ms. The microcontroller can then change the INIT registers and enter Normal mode (via SPI W/D refresh) within this allowed time frame; otherwise, the SBC will transition back into INIT Reset state as shown in Figure 73. The INIT phase is the only state where the INIT registers can be changed. If these are not changed, the default register values are taken. Refer to the datasheet for more details.

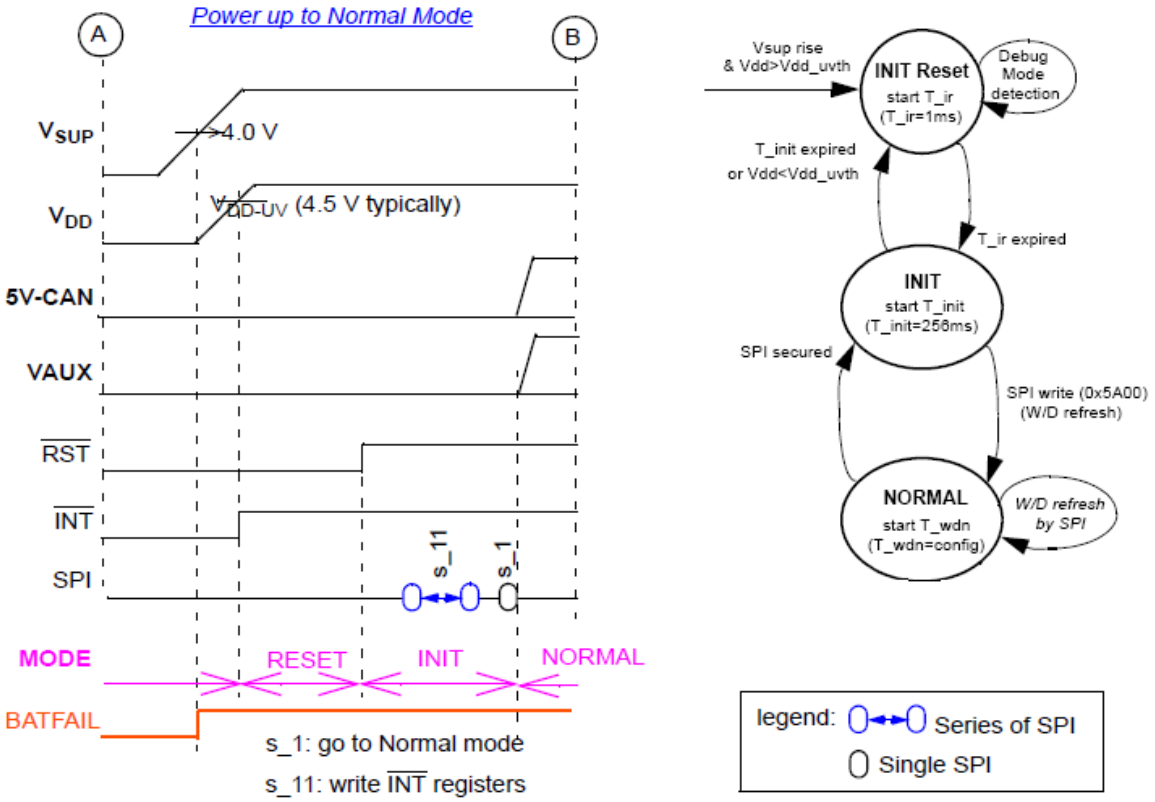


Figure 73. INIT reset, INIT, and normal mode after power up

There are four registers assigned for the initialization of the MC33903/4/5 SBC family, which are the INIT REG, INIT watchdog, INIT LIN I/O, and INIT MISC.

5.4.1 Initializing the regulators

The INIT REG register allows the microcontroller to initialize the cyclic sense functionality of I/O-1 to be dependent on I/O-0 activation or not and also the I/O-0 activation time. This register also allows the selection of the V_{DD} undervoltage threshold to trigger a $\overline{RST}$ and/or $\overline{INT}$ and the duration of the triggered reset after V_{DD} goes above the V_{DD} undervoltage threshold. The V_{AUX} voltage can also be initialized to 3.3 V or 5.0 V in this register.

Table 13. Initialization regulator registers, INIT REG (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0101 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 00 _ 101 P	I/O-x sync	V_{DDL} rst[1]	V_{DDL} rst[0]	V_{DD} rstD[1]	V_{DD} rstD[0]	V_{AUX}5/3	Cyclic on[1]	Cyclic on[0]
Default state	1	0	0	0	0	0	0	0
Condition for default	POR							

Bit	Description
b7	**I/O-x sync** - Determine if I/O-1 is sensed during I/O-0 activation, when cyclic sense function is selected
0	I/O-1 sense anytime
1	I/O-1 sense during I/O-0 activation
b6, b5	**$V_{DDL\ RST}$[1] $V_{DDL\ RST}$[0] -** Select the V_{DD} undervoltage threshold, to activate $\overline{RST}$ pin and/or INT

Bit	Description
00	Reset at approx 0.9 V_{DD}.
01	INT at approx 0.9 V_{DD}, Reset at approx 0.7 V_{DD}
10	Reset at approx 0.7 V_{DD}
11	Reset at approx 0.9 V_{DD}.
b4, b3	**$V_{DD\ RST}$D[1] $V_{DD\ RST}$D[0] - Select the $\overline{RST}$ pin low lev duration, after V_{DD} rises above the V_{DD} undervoltage threshold**
00	1.0 ms
01	5.0 ms
10	10 ms
11	20 ms
b2	**[V_{AUX} 5/3]** - Select Vauxilary output voltage
0	V_{AUX} = 3.3 V
1	V_{AUX} = 5.0 V
b1, b0	**Cyclic on[1] Cyclic on[0] - Determine I/O-0 activation time, when cyclic sense function is selected**
00	200 µs (typical value. Ref. to dynamic parameters for exact value)
01	400 µs (typical value. Ref. to dynamic parameters for exact value)
10	800 µs (typical value. Ref. to dynamic parameters for exact value)
11	1600 µs (typical value. Ref. to dynamic parameters for exact value)

5.4.2 Initializing the watchdog

The INIT watchdog register allows the microcontroller to initialize the SBC to implement advanced, window, or timeout watchdog operation. This register also allows for the initialization of the $\overline{SAFE}$ to be asserted after one or two consecutive resets. The maximum time delay between an $\overline{INT}$ assertion and the $\overline{INT}$ source read via the SPI can also be initialized in this register. For Low Power VDD ON mode, the overcurrent consumption and the deglitching time on VDD can be initialized to automatically wake-up with or without a watchdog refresh. The microcontroller is also allowed to initialize whether the V_{DD} is kept ON during a crank pulse or disabled when V_{SUP} goes below typ. 4.0 V.

Table 14. Initialization watchdog registers, INIT watchdog (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0110 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 00 _ 110 P	WD2INT	MCU_OC	OC-TIM	WD Safe	WD_spi[1]	WD_spi[0]	WD N/Win	Crank
Default state	0	1	0		0	0	1	0
Condition for default	POR							

Bit	Description
b7	**WD2INT -** Select the maximum time delay between INT occurrence and INT source read SPI command
0	Function disable. No constraint between INT occurrence and INT source read.

Bit	Description
1	INT source read must occur before the remaining of the current watchdog period plus 2 complete watchdog periods.
b6, b5	**MCU_OC, OC-TIM -** In LP V_{DD} ON, select watchdog refresh and V_{DD} current monitoring functionality. $V_{DD\_OC\_LP}$ threshold is defined in device electrical parameters (approx 1.5 mA)
	In LP mode, when watchdog is not selected
no watchdog + 00	In LP V_{DD} ON mode, V_{DD} overcurrent has no effect
no watchdog + 01	In LP V_{DD} ON mode, V_{DD} overcurrent has no effect
no watchdog + 10	In LP V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > 100 µs (typically) is a wake-up event
no watchdog + 11	In LP V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is a wake-up event. I_mcu_OC time is selected in Timer register (selection range from 3.0 to 32 ms)
	In LP mode when watchdog is selected
watchdog + 00	In LP V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. watchdog refresh must occur by SPI command.
watchdog + 01	In LP V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. watchdog refresh must occur by SPI command.
watchdog + 10	In LP V_{DD} ON mode, V_{DD} overcurrent for a time > 100 µs (typically) is a wake-up event.
watchdog + 11	In LP V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time < I_mcu_OC is a watchdog refresh condition. V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is a wake-up event. I_mcu_OC time is selected in Timer register (selection range from 3.0 to 32 ms)
b4	**WD Safe -** Select the activation of the SAFE pin low, at first or second consecutive RESET pulse
0	SAFE pin is set low at the time of the $\overline{RST}$ pin low activation
1	SAFE pin is set low at the second consecutive time $\overline{RST}$ pulse
b3, b2	**WD_spi[1] WD_spi[0] -** Select the Watchdog (watchdog) Operation
00	Simple Watchdog selection: watchdog refresh done by a 8 bits or 16 bits SPI
01	Enhanced 1: Refresh is done using the Random Code, and by a single 16 bits.
10	Enhanced 2: Refresh is done using the Random Code, and by two 16 bits command.
11	Enhanced 4: Refresh is done using the Random Code, and by four 16 bits command.
b1	**WD N/Win -** Select the Watchdog (watchdog) Window or Timeout operation
0	Watchdog operation is TIMEOUT, watchdog refresh can occur anytime in the period
1	Watchdog operation is WINDOW, watchdog refresh must occur in the open window (second half of period)
b0	**Crank -** Select the $V_{SUP/1}$ threshold to disable V_{DD}, while V_{SUP1} is falling toward GND
0	V_{DD} disable when $V_{SUP/1}$ is below typically 4.0 V (parameter $V_{SUP\text{-}TH1}$), and device in Reset mode
1	V_{DD} kept ON when $V_{SUP/1}$ is below typically 4.0 V (parameter V_{SUP_TH1})

5.4.3 Initializing the LIN and I/O

The INIT LIN I/O register allows the microcontroller to initialize the I/Os as inputs, high-side or low-side outputs, or LIN termination switches. Additionally, I/O-1 can be initialized to be automatically turned OFF as a result of an overvoltage condition on VDD or Vaux. This register also allows the initialization of I/O-0 to be disabled or inversely enabled during cyclic sense wake-up functionality.

Table 15. Initialization LIN and I/O registers, INIT LIN I/O (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0111 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 00 _ 111 P	I/O-1 ovoff	LIN_T2[1]	LIN_T2[0]	LIN_T/1[1]	LIN_T/1[0]	I/O-1 out-en	I/O-0 out-en	Cyc_Inv
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	Description
b7	**I/O-1 ovoff -** Select the deactivation of I/O-1 when V_{DD} or V_{AUX} overvoltage condition is detected
0	Disable I/O-1 turn off.
1	Enable I/O-1 turn off, when V_{DD} or V_{AUX} overvoltage condition is detected.
b6, b5	**LIN_T2[1], LIN_T2[0]** - Select pin operation as LIN Master pin switch or I/O
00	pin is OFF
01	pin operation as LIN Master pin switch
10	pin operation as I/O: HS switch and Wake-up input
11	N/A
b4, b3	**LIN_T/1[1], LIN_T/1[0] -** Select pin operation as LIN Master pin switch or I/O
00	pin is OFF
01	pin operation as LIN Master pin switch
10	pin operation as I/O: HS switch and Wake-up input
11	N/A
b2	**I/O-1 out-en**- Select the operation of the I/O-1 as output driver (HS, LS)
0	Disable HS and LS drivers of pin I/O-1. I/O-1 can only be used as input.
1	Enable HS and LS drivers of pin I/O-1. Pin can be used as input and output driver.
b1	**I/O-0 out-en -** Select the operation of the I/O-0 as output driver (HS, LS)
0	Disable HS and LS drivers of I/O-0 can only be used as input.
1	Enable HS and LS drivers of the I/O-0 pin. Pin can be used as input and output drivers.
b0	**Cyc_Inv -** Select I/O-0 operation in device LP mode, when cyclic sense is selected

Bit	Description
0	During cyclic sense active time, I/O is set to the same state prior to entering in to LP mode. During cyclic sense off time, I/O-0 is disable (HS and LS drivers OFF).
1	During cyclic sense active time, I/O is set to the same state prior to entering in to LP mode. During cyclic sense off time, the opposite driver of I/O_0 is actively set. Example: If I/0_0 HS is ON during active time, then I/O_O LS is turned ON at expiration of the active time, for the duration of the cyclic sense period.

5.4.4 Initializing miscellaneous functions

The INIT MISC register allows the microcontroller to initialize various functions of the SBC. Going into Low Power mode VDD ON or OFF can be initialized to enable bits 2, 1, and 0 of the MODE register to serve as conditional random bits for the transition from Normal to either of the Low Power modes to occur. Note that the random bits of the SPI write command sent to the MODE register to go into Low Power mode must be the complement of the random bits; otherwise, the message is ignored and SBC stays in Normal mode.

The INIT MISC also allows for the initialization to enable or disable SPI parity implementation. Additionally, the INT pulse duration can be initialized when selected as a pulse or the INT can be initialized to be a permanent 'low' assertion. This register also allows for the initialization to optionally get an INT pulse during Flash mode at 50% of the watchdog period.

This register also allows flexibility to verify and modify the $\overline{\text{SAFE}}$ output operation via the SPI command in addition to the hardware configuration (resistor value on DBG pin).

Table 16. Initialization miscellaneous functions, INIT MISC (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_1000 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 000 P	LPM w RNDM	SPI parity	INT pulse	INT width	INT flash	Dbg Res[2]	Dbg Res[1]	Dbg Res[0]
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	Description
b7	**LPM w RNDM -** This enables the usage of random bits 2, 1 and 0 of the MODE register to enter into LP VDD OFF or LP VDD ON.
0	Function disable: the LP mode can be entered without usage of Random Code
1	Function enabled: the LP mode is entered using the Random Code
b6	**SPI parity -** Select usage of the parity bit in SPI write operation
0	Function disable: the parity is not used. The parity bit must always set to logic 0.
1	Function enable: the parity is used, and parity must be calculated.
b5	**INT pulse -**Select INT pin operation: low level pulse or low level
0	INT pin will assert a low level pulse, duration selected by bit [b4]
1	INT pin assert a permanent low level (no pulse)
b4	**INT width -** Select the INT pulse duration
0	INT pulse duration is typically 100 µs. Ref. to dynamic parameter table for exact value.
1	INT pulse duration is typically 25 µs. Ref. to dynamic parameter table for exact value.

Bit	Description
b3	**INT flash -** Select INT pulse generation at 50% of the Watchdog Period in Flash mode
	Function disable
	Function enable: an INT pulse will occur at 50% of the Watchdog Period when device in Flash mode.
b2, b1, b0	**Dbg Res[2], Dbg Res[1], Dbg Res[0] -** Allow verification of the external resistor connected at DBG pin. Ref. to parametric table for resistor range value.
0xx	Function disable
100	100 verification enable: resistor at DBG pin is typically 68 kΩ (RB3) - Selection of SAFE mode B3
101	101 verification enable: resistor at DBG pin is typically 33 kΩ (RB2 - Selection of SAFE mode B2
110	110 verification enable: resistor at DBG pin is typically 15 kΩ (RB1) - Selection of SAFE mode B1
111	111 verification enable: resistor at DBG pin is typically 0 kΩ (RA) - Selection of SAFE mode A

5.5 Watchdog operation

There are three different watchdog types available when working with the MC33903/4/5 family of SBCs. The well known common types available for these SBCs are the simple 'timeout' and 'window' watchdog. Additionally, the MC33903/4/5 enhances functional safety robustness by offering an 'advanced' watchdog, which includes three variation levels of security verification. The watchdog type is selected during the initialization phase of the SBC via the INIT Watchdog register (Table 14).

The transition from INIT or Normal Request mode into Normal mode only requires a single watchdog refresh command (0x5A00).

Once in Normal mode, the watchdog refresh SPI command is dependent on the watchdog type selected during the initialization phase of the SBC.

Important notice

Observation: it has been observed that RST or SAFE pin can be activated after a correct watchdog refresh SPI message. This behavior was observed only in a specific configuration.

- WD window set to 64 ms and WD refresh message sent every 40 ms (approx.)
- W/D setting is WINDOW, with single or ADVANCE configuration (refresh by multiple SPI messages)

Recommendations:

- Use a refresh period >41 ms, for example, close to 47 ms when a period of 64 ms with WD window setting is used, to further reduce the occurrence
- Use Timeout configuration: this setting will totally prevent the occurrence, for W/D refresh configuration by 1 or via multiple SPI messages
- To avoid SAFE pin activation with the first RST event, the “WD Safe” bit in the “INIT watchdog” register can be set to 1, and with this setting, the SAFE pin will be activated at the second consecutive RST event.

5.5.1 Simple watchdog

The watchdog refresh SPI command is 0x5A00 and it can be sent at any time within the watchdog period, if the SBC was initialized for timeout watchdog operation. The watchdog refresh command must be sent in the open window (second half of the period) if the SBC was initialized for window watchdog operation.

5.5.2 Advanced watchdog

The first time the SBC transitions into Normal mode via watchdog refresh SPI command 0x5A00, the Random (RNDM) code must be read using SPI command 0x1B00. The second byte of the RNDM code is then returned on MISO. The full 16 bits on MISO are called 0x XXRD, where RD is the complement of the RD byte (Refer to Table 17).

5.5.3 Advanced watchdog - refresh by one SPI command

The watchdog refresh command is 0x5ARD. During each refresh command the SBC will return a new Random Code on MISO. This new Random Code must be then be inverted and sent along with the next refresh command. This sequence must be done in an open window if the 'window' watchdog operation was selected during the initialization phase of the SBC (Refer to Table 17).

5.5.4 Advanced watchdog - refresh by two SPI commands

In this case, the refresh command is split into two SPI commands. The first partial refresh command is 0x5Aw1, and the second is 0x5Aw2. Byte w1 contains the first four inverted bits of the RD byte plus the last four bits equal to zero. Byte w2 contains four bits equal to zero plus the last four inverted bits of the RD byte.

During the second watchdog refresh command, the device returns a new Random Code on MISO. This new random code must then be inverted and sent along with the next two refresh commands and so on. The second command must be done in an open window if the 'window' watchdog operation was selected during the initialization phase of the SBC (Refer to Table 17).

5.5.5 Advanced watchdog - refresh by four SPI commands

In this case, the watchdog refresh command is split into four SPI commands.

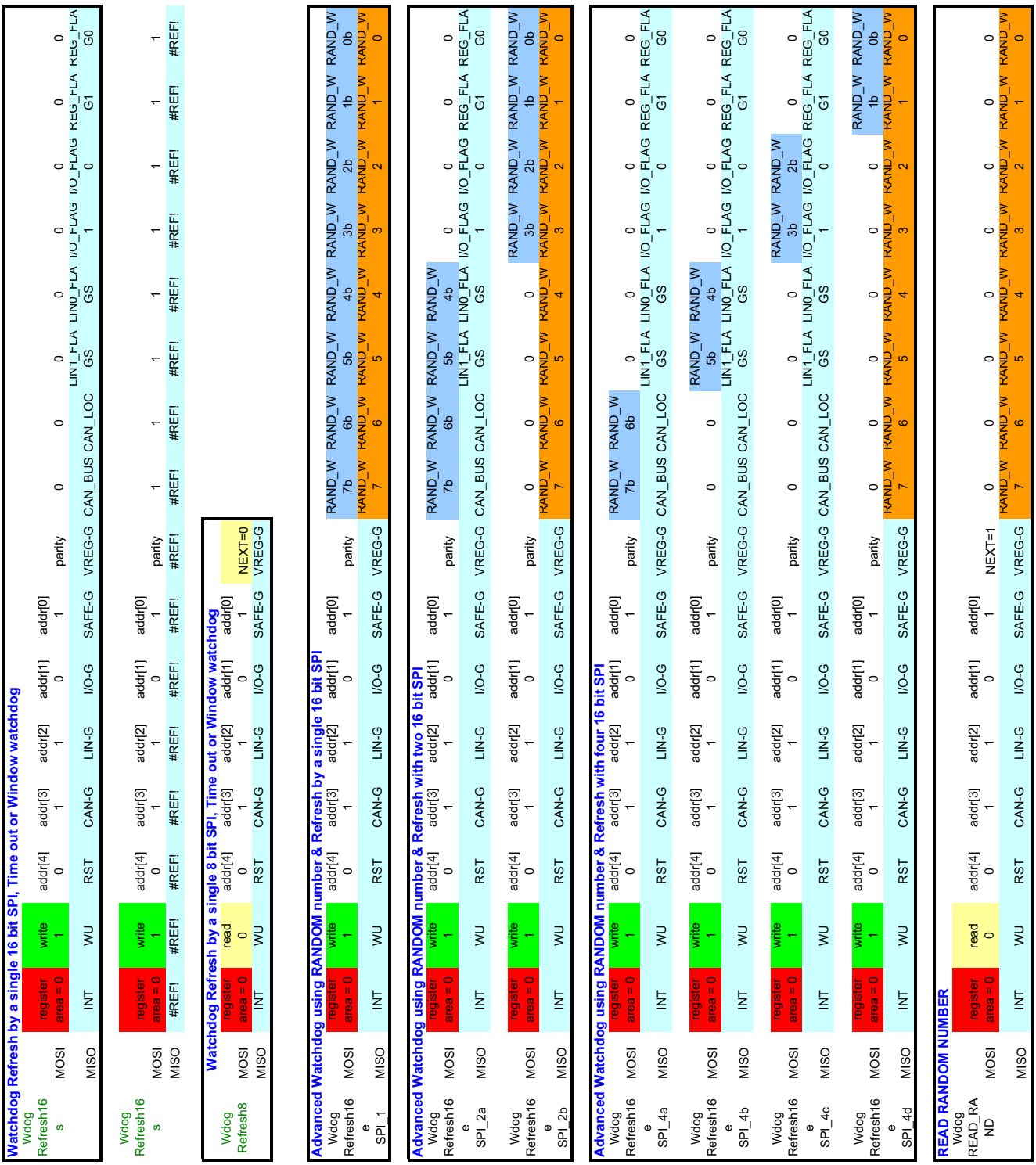
The first partial watchdog refresh command is 0x5Aw1, the second one is 0x5Aw2, the third one is 0x5Aw3, and the last one is 0x5Aw4.

- Byte w1 contains the first two inverted bits of the RD byte, plus the last six bits equal to zero.
- Byte w2 contains two bits equal to zero, plus the next two inverted bits of the RD byte, plus four bits equal to zero.
- Byte w3 contains four bits equal to zero, plus the next two inverted bits of the RD byte, plus two bits equal to zero.
- Byte w4 contains six bits equal to zero, plus the next two inverted bits of the RD byte.

During the fourth refresh command, the device will return a new Random Code on MISO. This new Random Code must be then be inverted and sent along with the next four refresh commands.

The fourth command must be done in an open window if the 'window' watchdog operation was selected during the initialization phase of the SBC (Refer to Table 17).

Table 17. Simple and enhanced watchdog



5.6 Normal mode

After all the initialization of the SBC is complete, the transition to normal mode can then take place. To go to normal mode from the INIT or Normal Request states, the SBC must receive a watchdog refresh from the microcontroller. The specific hex SPI command is 0x5A00. Once in Normal mode, the watchdog must be refreshed (unless Debug mode is activated) according to watchdog type selected during the initialization of the SBC. If there is a missing or incorrect watchdog, the SBC will automatically go into Reset mode. All of the MC33903/4/5 functions are available during normal mode and the SBC can transition to Low power VDD ON and Low Power VDD OFF with a typical SPI command. Additionally, the SBC can transition into Flash, Reset, or back into Initialization mode via Secured SPI command.

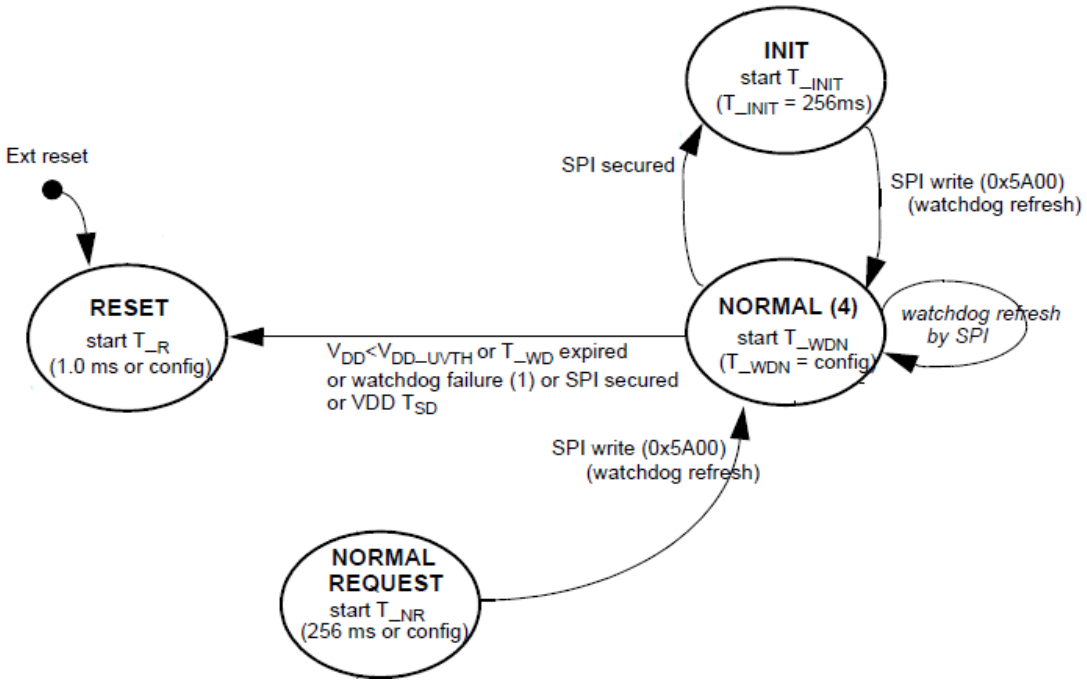


Figure 74. INIT, normal, normal request, and reset state diagram

5.6.1 Timers

The MC33903/4/5 family of SBCs provides the module designer with flexibility to configure several timers of the SBC during critical modes such as Flash and Reset. Additionally, the window or timeout watchdog period can be adjusted according to the module's microcontroller requirements. During Low Power modes, there are various timing parameters that can also be configured to meet the module's functional safety and current consumption requirements.

During Normal mode operation of the SBC, the watchdog period is set to 256 ms by default, but can be modified accordingly via bits b4 and b3 in the Timer Register A. This period can be doubled to 512 ms or shortened all the way down to 2.5 ms dependent on module and microcontroller timing requirements (refer to Table 18).

Table 18. Timer register A, LP V_{DD} overcurrent and watchdog period normal mode, TIM_A

MOSI First Byte [15-8] [b_15 b_14] 01_010 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 010 P	I_mcu[2]	I_mcu[1]	I_mcu[1]	watchdog Nor[4]	W/D_N[4]	W/D_Nor[3]	W/D_N[2]	W/D_Nor[0]
Default state	0	0	0	1	1	1	1	0
Condition for default	POR							

LP V_{DD} overcurrent (ms)				
b7	b6, b5			
	00	01	10	11
0	3 (def)	6	12	24
1	4	8	16	32

Watchdog period in device normal mode (ms)								
b4, b3	b2, b1, b0							
	000	001	010	011	100	101	110	111
00	2.5	5	10	20	40	80	160	320
01	3	6	12	24	48	96	192	384
10	3.5	7	14	28	56	112	224	448
11	4	8	16	32	64	128	256 (def)	512

The MC33903/4/5 will allow micro amps of current to be drawn by the microcontroller during Low power VDD ON mode. If the current consumption on VDD exceeds a minimum of 1.0 mA and lasts longer than the configured amount of time in Timer Register A, the SBC will wake up and trigger an Interrupt. The time for which the current consumption may last is configurable from 3.0 ms (default) up to 32 ms dependent on bits b7, b6, and b5. Refer to Table 18.

When in Low Power VDD ON mode, the SBC can be configured to cyclically interrupt the microcontroller. The Interruption period can be configured from 6ms (default) up to 1s dependent on bits b3, b2, b1, and b0 of the Timer Register B (refer to Table 19).

Table 19. Timer register B, cyclic sense and cyclic INT, in device LP mode, TIM_B

MOSI First Byte [15-8] [b_15 b_14] 01_011 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 011 P	Cyc-sen[3]	Cyc-sen[2]	Cyc-sen[1]	Cyc-sen[0]	Cyc-int[3]	Cyc-int[2]	Cyc-int[1]	Cyc-int[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Cyclic Sense (ms)								
b7	b6, b5, b4							
	000	001	010	011	100	101	110	111
0	3	6	12	24	48	96	192	384
1	4	8	16	32	64	128	256	512

Cyclic Interrupt (ms)								
b3	b2, b1, b0							
	000	001	010	011	100	101	110	111
0	6 (def)	12	24	48	96	192	384	768
1	8	16	32	64	128	258	512	1024

During Low Power VDD ON and OFF, the SBC can be configured to cyclically pulse I/O-0 to monitor the rest of the I/Os for a change of state as described in Figure 84. The cyclic I/O pulse period can be configured from 3.0 ms (default) up to 512 ms dependent on bits b7, b6, b5, and b4 of the Timer Register B (refer to Table 19). Additionally, a Forced Wake-up timer can be configured to automatically wake-up the SBC after the specified amount of time has elapsed according to bits b3, b2, b1, and b0 configuration in Timer Register C. The Forced Wake-up period can be configured from 48 ms (default) up to eight seconds. Refer to Table 20.

Table 20. Timer Register C, Watchdog LP Mode or Flash Mode and Forced Wake-up Timer, TIM_C

MOSI First Byte [15-8] [b_15 b_14] 01_100 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 100 P	WD-LP-F[3]	WD-LP-F[2]	WD-LP-F[1]	WD-LP-F[0]	FWU[3]	FWU[2]	FWU[1]	FWU[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Watchdog in LP V_{DD} ON Mode (ms)								
b7	**b6, b5, b4**							
	000	001	010	011	100	101	110	111
0	12	24	48	96	192	384	768	1536
1	16	32	64	128	256	512	1024	2048
Watchdog in Flash Mode (ms)								
b7	**b6, b5, b4**							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	256	512	1024	2048	4096	8192	16384	32768
Forced Wake-up (ms)								
b3	**b2, b1, b0**							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	64	128	258	512	1024	2048	4096	8192

The watchdog period for Flash mode operation can be configured to 48 ms (default) and extended up to 32 seconds dependent on bits b7, b6, b5, and b4 setting in Timer Register C (refer to Table 20). This allows the sufficient amount of time for the flashing of the module and provides flexibility to fulfill timing requirements.

During Low Power VDD ON mode, the microcontroller is active with low current capability. Typically, the watchdog refresh operation is not required during Low Power modes, but the MC33903/4/5 provides the flexibility to include the added safety of enabling the watchdog operation during Low Power VDD ON mode. The watchdog period can be set from 12 ms (default) up to two seconds dependent on bits b7, b6, b5, and, b4 configuration in Timer Register C. Refer to Table 20.

5.6.2 Continuous monitoring of supplies

The MC33903/4/5 family of SBCs includes various embedded regulators that are supplied from the VSUP1 and VSUP2 input pins. Additionally, the SBC has a VSENSE input, which can be connected directly to the battery line via a 1.0 kΩ resistor. During Normal mode, there is continuous monitoring of the embedded regulators for the SBC to meet functional safety module specifications such as keeping regulator ON regardless of a fault or optionally protecting itself by shutting down.

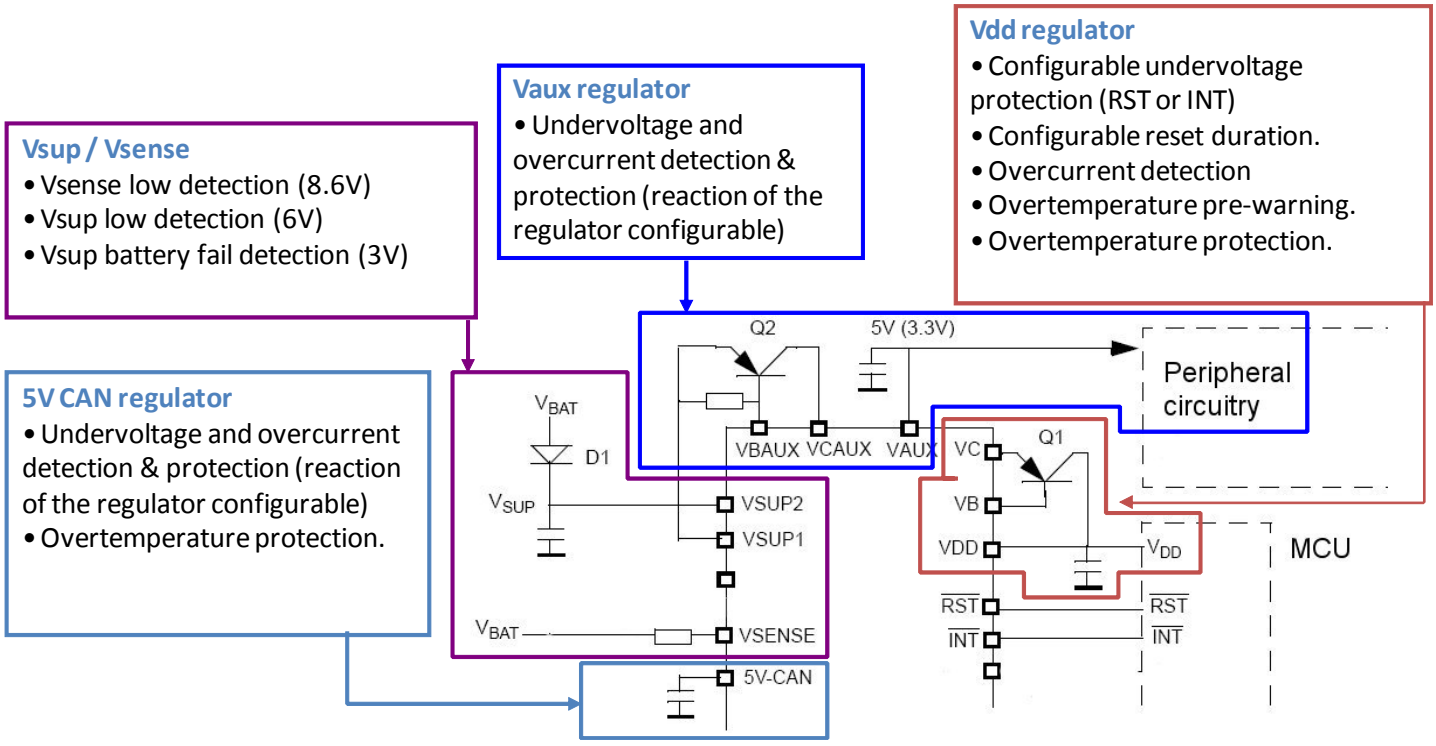


Figure 75. Supply monitoring

Any faults on the VDD regulator causing it to fall below the specified datasheet threshold will automatically trigger a $\overline{RST}$ or both a $\overline{RST}$ and an $\overline{INT}$ depending on how it was initialized via bits b6 and b5 in the INIT REG register (see Table 21).

Table 21. Initialization the VDD regulator

MOSI First Byte [15-8] [b_15 b_14] 0_0101 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 00 _ 101 P	I/O-x sync	V_{DDL} rst[1]	V_{DDL} rst[0]	V_{DD} rstD[1]	V_{DD} rstD[0]	V_{AUX}5/3	Cyclic on[1]	Cyclic on[0]
Default state	1	0	0	0	0	0	0	0
Condition for default	POR							

Bit	Description
b6, b5	**$V_{DDL\ RST}$[1] $V_{DDL\ RST}$[0] -** Select the V_{DD} undervoltage threshold, to activate $\overline{RST}$ pin and/or INT
00	Reset at approx 0.9 V_{DD}.
01	INT at approx 0.9 V_{DD}, Reset at approx 0.7 V_{DD}
10	Reset at approx 0.7 V_{DD}
11	Reset at approx 0.9 V_{DD}.

The Vsup/1 voltage can be monitored by the microcontroller via the multiplexer (MUX-OUT) output connected to the microcontroller's A/D converter. Additionally, If the VSUP1 pin voltage goes below typically 6.0 V, a flag is set and the corresponding bit1 ($V_{SUP\_UNDERVOLTAGE}$) is latched in the REG flags register (shown on Table 22). As with any flag, once the SBC has recovered from the failure, the flag can then be cleared by reading the corresponding register. Any time the Vsup/1 voltage drops below typically 3.0 V, the $V_{SUP\_BATFAIL}$ bit in the REG flag register is set. If the VSENSE pin voltage drops below typically 8.6 V, a flag is set for its corresponding bit2 (V_{SENSE_LOW}).

Note: The $\overline{RST}$ pin is guaranteed to remain triggered 'low' all the way down to a minimum VSUP1 voltage of 2.5 V.

Table 22. Supply and regulator flags

Bits	15-14	13-9	8	7	6	5	4	3	2	1	0
MOSI	MOSI bits 15-7				Next 7 MOSI bits (bits 6.0) should be “000_0000”						
	bits [15, 14]	Address [13-9]	bit 8	bit 7							
MISO	8 Bits Device Fixed Status (bits 15...8)				MISO bits [7-0], device response on MISO pin						
					bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REG	11	0_1111 REG	1	0	V_{AUX_LOW}	$V_{AUX\_overCURRENT}$	$5V_{-CAN\_}$ THERMAL SHUTDOWN	$5V_{-CAN\_}$ UV	$5V_{-CAN\_}$ overCURRENT	$V_{SENSE\_}$ LOW	$V_{SUP\_}$ underVOLTAGE	$I_{DD-OC-NORMAL\ MODE}$
	11			1	-	-	-	$V_{DD\_}$ THERMAL SHUTDOWN		R_{ST_LOW} (<100 ms)	$V_{SUP\_}$ BATFAIL	$I_{DD-OC-LP}$ V_{DD}ON MODE
	Hexa SPI commands to get Vreg Flags: MOSI 0x DF 00, and MOSI Ox DF 80											

The VAUX and 5V_CAN regulators can also be continuously monitored by the microcontroller via the REG flags register and the response to any faults can be configured via the Regulator Register (Refer to Table 23 for more details).

Table 23. Regulator register

MOSI First Byte [15-8] [b_15 b_14] 01_111 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 111 P	V_{AUX}[1]	V_{AUX}[0]	-	5V-can[1]	5V-can[0]	V_{DD} bal en	V_{DD} bal auto	V_{DD} OFF en
Default state	0	0	N/A	0	0	N/A	N/A	N/A
Condition for default	POR			POR				

Bits	Description
b7 b6	**V_{AUX}[1], V_{AUX}[0]** - Vauxilary regulator control
00	Regulator OFF
01	Regulator ON. Undervoltage (UV) and overcurrent (OC) monitoring flags not reported. V_{AUX} is disabled when UV or OC detected after 1.0 ms blanking time.
10	Regulator ON. Undervoltage (UV) and overcurrent (OC) monitoring flags active. V_{AUX} is disabled when UV or OC detected after 1.0 ms blanking time.
11	Regulator ON. Undervoltage (UV) and overcurrent (OC) monitoring flags active. V_{AUX} is disabled when UV or OC detected after 25 µs blanking time.
b4 b3	**5 V-can[1], 5 V-can[0]** - 5V-CAN regulator control
00	Regulator OFF

Bits	Description
01	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags not reported. 1.0 ms blanking time for UV and OC detection. Note: by default when in Debug mode
10	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags active. 1.0 ms blanking time for UV and OC detection.
11	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags active after 25 µs blanking time.
b2	**V_{DD} bal en** - Control bit to Enable the V_{DD} external ballast transistor
0	External V_{DD} ballast disable
1	External V_{DD} ballast Enable
b1	**V_{DD} bal auto -** Control bit to automatically Enable the V_{DD} external ballast transistor, if V_{DD} is > typically 60 mA
0	Disable the automatic activation of the external ballast
1	Enable the automatic activation of the external ballast, if V_{DD} > typically 60 mA
b0	**V_{DD} OFF en -** Control bit to allow transition into LP V_{DD} OFF mode (to prevent V_{DD} turn OFF)
0	Disable Usage of LP V_{DD} OFF mode
1	Enable Usage of LP V_{DD} OFF mode

Bits b7 and b6 of the Regulator register allow for the Vaux regulator to be configured to enable or disable undervoltage and overcurrent monitoring. When the monitoring is enabled, the V_{AUX} can be configured to either automatically turn OFF or stay ON in case of a fault.

Bits b4 and b3 of the Regulator register allow for the 5V-CAN regulator to be configured to enable or disable undervoltage and overcurrent monitoring. When the monitoring is enabled, the V_{AUX} can be configured to either automatically turn OFF or stay ON in case of a fault.

Bits b2 and b1 allow for external ballast transistor to be forced enabled, disabled, or to automatically be enabled in case of higher current draw on V_{DD}.

Note: Bit b0 is critical because it must be set in order for the SBC to be allowed to transition into Low Power VDD OFF mode. This is to make sure the SBC does not transition into Low Power VDD OFF by accident.

5.6.3 Multiplexer capability

Some of the MC33903/4/5 SBC devices also implement a multiplexed output (MUX-OUT), where critical voltages and other parameters of the SBC can be measured to implement a functional safe and robust system. The output voltage of this pin is limited to the SBC's VDD voltage. Bits b7, b6, and b5 allow the microcontroller to select which parameter to measure out on MUX-OUT, which should be connected to the A/D converter. Depending on bit configuration, the VSENSE voltage, VSUP1 voltage, I/O-1 voltage, I/O-0 voltage, SBC silicon temperature, internal 2.5 V reference, or the VDD current re-copy can be selected to be read on the multiplexed output pin (MUX-OUT). Bit b4 allows the selection of an internal 2.0KΩ resistor to measure V_{DD} current re-copy in lieu of a higher accuracy external resistor that can be optionally placed on MUX-OUT. Note that this resistor is only required if the V_{DD} output current needs to be measured. Bit b3 allows the attenuation or gain of the I/O-0 or I/O-1 voltage inputs. The attenuation allows for I/O-0 and I/O-1 voltages up to 16 V to be accurately measured by the A/D converter of the microcontroller. The gain functionality allows the microcontroller to accurately read much lower voltages, which do not exceed 2.5 V on the I/O-0 and I/O-1 inputs.

Note: The MUX register can be written and read only when the 5V-CAN regulator is ON; otherwise, the SPI command sent is ignored and the MUX register content is reset to its default state.

Table 24. MUX register

MOSI First Byte [15-8] [b_15 b_14] 0_0000 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 00 _ 000 P	MUX_2	MUX_1	MUX_0	Int 2K	I/O-att	0	0	0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR, 5 V-CAN off, any mode different from Normal							

Bits	Description
b7 b6 b5	**MUX_2, MUX_1, MUX_0** - Selection of external input signal or internal signal to be measured at MUX-OUT pin
000	All functions disable. No output voltage at MUX-OUT pin
001	V_{DD} regulator current recopy. Ratio is approx 1/97. Requires an external resistor or selection of Internal 2.0 K (bit 3)
010	Device internal voltage reference (approx 2.5 V)
011	Device internal temperature sensor voltage
100	Voltage at I/O-0. Attenuation or gain is selected by bit 3.
101	Voltage at I/O-1. Attenuation or gain is selected by bit 3.
110	Voltage at VSUP/1 pin. Refer to electrical table for attenuation ratio (approx 5)
111	Voltage at VSENSE pin. Refer to electrical table for attenuation ratio (approx 5)
b4	**INT 2k** - Select device internal 2.0 kΩ resistor between AMUX and GND. This resistor allows the measurement of a voltage proportional to the V_{DD} output current.
0	Internal 2.0 kΩ resistor disable. An external resistor must be connected between AMUX and GND.
1	Internal 2.0 kΩ resistor enable.
b3	**I/O-att** - When I/O-0 (or I/O-1) is selected with b7,b6,b5 = 100 (or 101), b3 selects attenuation or gain between I/O-0 (or I/O-1) and MUX-OUT pin
0	Gain is approx 2 for device with V_{DD} = 5.0 V (Ref. to electrical table for exact gain value) Gain is approx 1.3 for device with V_{DD} = 3.3 V (Ref. to electrical table for exact gain value)
1	Attenuation is approx 4 for device with V_{DD} = 5.0 V (Ref. to electrical table for exact attenuation value) Attenuation is approx 6 for device with V_{DD} = 3.3 V (Ref. to electrical table for exact attenuation value)

If the optional >2.0 kΩ external resistor to GND on MUX-OUT to read VDD current re-copy is implemented, the maximum MUX-OUT voltage will be VDD-0.5 V. Optionally, an internal resistor can be selected via the SPI, but the accuracy is decreased as specified in Table 25. If the optional capacitor on the MUX-OUT pin is implemented it should not exceed 1.0 nF. The voltage reading on the multiplexed output for the chip temperature and the internal reference voltage directly corresponds to the parameter measured as specified in Table 25. When measuring VSENSE voltage, the voltage on MUX-OUT has to be multiplied by typically 5.48 or 8.2 depending on V_{DD} voltage. When measuring V_{SUP1} voltage, the voltage on MUX-OUT has to be multiplied by typically 5.5 or 8.18 depending on V_{DD} voltage. When measuring I/O-0 or I/O-1 voltage with attenuation (ranging from 0 V - 16 V), the reading on MUX-OUT has to be multiplied by typically 4 or 5.8 depending on V_{DD} voltage. When measuring I/O-0 or I/O-1 voltage (ranging from 0 V - 2.5 V), the reading on MUX-OUT has to be multiplied by typically 2 or 1.3 depending on VDD voltage. To measure the VDD current, the voltage reading on MUX-OUT must be divided by the resistance value (internally selected or externally populated) and then multiplied by typically 97. See Table 25 for accurate parametric measurement ranges.

Table 25. Multiplexer

Characteristic	Symbol	Min.	Typ.	Max.	Unit
ANALOG MUX OUTPUT					
Output Voltage Range, with external resistor to GND >2.0 kΩ	V_{OUT_MAX}	0.0	-	V_{DD} - 0.5	V
Internal pull-down resistor for regulator output current sense	R_{MI}	0.8	1.9	2.8	kΩ
External capacitor at MUX OUTPUT (Guaranteed by design)	C_{MUX}	-	-	1.0	nF
Chip temperature sensor coefficient (Guaranteed by design and device characterization) V_{DD} = 5.0 V V_{DD} = 3.3 V	$TEMP_{-COEFF}$	 20 13.2	 21 13.9	 22 14.6	mv/°C
Chip temperature: MUX-OUT voltage V_{DD} = 5.0 V, T_A = 125 °C V_{DD} = 3.3 V, T_A = 125 °C	V_{TEMP}	 3.6 2.45	 3.75 2.58	 3.9 2.65	V

Table 25. Multiplexer (continued)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Chip temperature: MUX-OUT voltage (guaranteed by design and characterization) T_A = -40 °C, V_{DD} = 5.0 V T_A = 25 °C, V_{DD} = 5.0 V T_A = -40 °C, V_{DD} = 3.3 V T_A = 25 °C, V_{DD} = 3.3 V	$V_{TEMP(GD)}$	 0.12 1.5 0.07 1.08	 0.30 1.65 0.19 1.14	 0.48 1.8 0.3 1.2	V
Gain for V_{SENSE}, with external 1.0 k 1% resistor V_{DD} = 5.0 V V_{DD} = 3.3 V	V_{SENSE} GAIN	 5.42 8.1	 5.48 8.2	 5.54 8.3	
Offset for V_{SENSE}, with external 1.0 k 1% resistor	$V_{SENSE\ OFFSET}$	-20	-	20	mV
Divider ratio for $V_{SUP/1}$ V_{DD} = 5.0 V V_{DD} = 3.3 V	$V_{SUP/1}$ RATIO	 5.335 7.95	 5.5 8.18	 5.665 8.45	
Attenuation/Gain ratio for I/O-0 and I/O-1 actual voltage: V_{DD} = 5.0 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1) V_{DD} = 5.0 V, (Gain, MUX-OUT register bit 3 set to 0) V_{DD} = 3.3 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1) V_{DD} = 3.3 V, (Gain, MUX-OUT register bit 3 set to 0)	VI/O RATIO	 3.8 - 5.6 -	 4.0 2.0 5.8 1.3	 4.2 - 6.2 -	
Internal reference voltage V_{DD} = 5.0 V V_{DD} = 3.3 V	V_{REF}	 2.45 1.64	 2.5 1.67	 2.55 1.7	V
Current ratio between VDD output & I_{OUT} at MUX-OUT (I_{OUT} at MUX-OUT = I_{DD} out / I_{DD_RATIO}) At I_{OUT} = 50 mA $I_{\_OUT}$ from 25 to 150 mA	I_{DD_RATIO}	 80 62.5	 97 97	 115 117	

5.6.4 Exercising the I/Os

All of the MC33903/4/5 SBCs have one to four configurable I/Os. These can be enabled and disabled in the I/O Register according to how they were initialized. Bits b7 and b6 allow I/O-3 to be high-impedance disabled with no wake-up capability, high-impedance disabled with wake-up capability (default by SAFE mode), or enabled as a high-side output at VSUP1 voltage. Bits b5 and b4 allow I/O-2 to be high-impedance disabled with no wake-up capability, high-impedance disabled with wake-up capability (default by SAFE mode), or enabled as a high-side output at V_{SUP1} voltage. Bits b3 and b2 allow I/O-1 to be high-impedance disabled with no wake-up capability, high impedance disabled with wake-up capability (default by SAFE mode), or enabled as a high-side or low-side output at V_{SUP1} voltage or GND correspondingly (also available in Low Power mode, but protection is disabled). Bits b1 and b0 allow I/O-0 to be high-impedance disabled with no wake-up capability, high-impedance disabled with wake-up capability (default by SAFE mode), or enabled as a high-side or low-side output at V_{SUP1} voltage or GND correspondingly (also available in Low Power mode, but protection is disabled). See Table 26.

Note: I/O-3 and I/O-2 may optionally be initialized as LIN-T2 and LIN-T1 correspondingly. In this case, the state of these must be controlled in the LIN/1 and LIN2 Registers.

Table 26. I/O register

MOSI First byte [15-8] [b_15 b_14] 10_001 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 001P	I/O-3 [1]	I/O-3 [0]	I/O-2 [1]	I/O-2 [0]	I/O-1 [1]	I/O-1 [0]	I/O-0 [1]	I/O-0 [0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	Description
b7 b6	I/O-3 [1], I/O-3 [0] - I/O-3 pin operation
00	I/O-3 driver disable, Wake-up capability disable
01	I/O-3 driver disable, Wake-up capability enable.
10	I/O-3 HS driver enable.
11	I/O-3 HS driver enable.
b5 b4	I/O-2 [1], I/O-2 [0] - I/O-2 pin operation
00	I/O-2 driver disable, Wake-up capability disable
01	I/O-2 driver disable, Wake-up capability enable.
10	I/O-2 HS driver enable.
11	I/O-2 HS driver enable.
b3 b2	I/O-1 [1], I/O-1 [0] - I/O-1 pin operation
00	I/O-1 driver disable, Wake-up capability disable
01	I/O-1 driver disable, Wake-up capability enable.
10	I/O-1 LS driver enable.
11	I/O-1 HS driver enable.
b1 b0	I/O-0 [1], I/O-0 [0] - I/O-0 pin operation
00	I/O-0 driver disable, Wake-up capability disable
01	I/O-0 driver disable, Wake-up capability enable.
10	I/O-0 LS driver enable.
11	I/O-0 HS driver enable.

5.6.5 Masking and enabling interrupts

There are multiple events that may trigger an interrupt to the microcontroller, which could be masked by the SBC dependent on module requirements. As shown in Table 27, a CAN, LIN1, LIN2, or I/O failure may trigger an INT depending on INT Register configuration. Additionally, the microcontroller can request an INT when desired by setting bits b6 AND b2. An interrupt may also be configured to trigger in the event of a fault on VAUX, VDD, RST or a SAFE resistor mismatch via bit b2. Continuous monitoring on Vaux, 5V-CAN, and VDD also allows for configurable INT triggering via bit b0.

Note: All bits in the INT Register are disabled by default.

Table 27. INT Register

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 010P	CAN failure	MCU req	LIN2 fail	LIN1fail	I/O	SAFE	-	Vmon
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	Description
b7	**CAN failure** - control bit for CAN failure INT (CANH/L to GND, VDD or VSUP, CAN overcurrent, Driver Overtemp, TXD-PD, RXD-PR, RX2HIGH, and CANBUS Dominate clamp)
0	INT disable
1	INT enable.
b6	MCU req - Control bit to request an INT. INT will occur once when the bit is enable
0	INT disable
1	INT enable.
b5	**LIN2 fail** - Control bit to enable INT when of failure on LIN2 interface
0	INT disable
1	INT enable.
b4	**LIN/1 fail** - Control bit to enable INT when of failure on LIN1 interface
0	INT disable
1	INT enable.
b3	**I/O** - Bit to control I/O interruption: I/O failure
0	INT disable
1	INT enable.
b2	**SAFE** - Bit to enable INT when of: Vaux overvoltage, VDD overvoltage, VDD Temp pre-warning, VDD undervoltage, SAFE resistor mismatch, RST terminal short to VDD, MCU request INT.
0	INT disable
1	INT enable.
b0	**V_{MON}** - enable interruption by voltage monitoring of one of the voltage regulator: V_{AUX}, 5 V-CAN, V_{DD} (I_{DD} Overcurrent, V_{SUV}, V_{SOV}, $V_{SENSELOW}$, 5V-CAN low or thermal shutdown, V_{AUX} low or V_{AUX} overcurrent
0	INT disable
1	INT enable.

5.6.6 RAM

The MC33903/4/5 SBC includes four different memory bytes that can be used to store values depending on module requirements. Memory bytes A, B, C, and D are each made up of 8 bits as shown in Table 28.

One benefit of having this RAM available is to be able to generate a longer duration timer than the longest Forced Wake-up time (8 seconds) available for example. A value can be stored in RAM in order to be able to count more than 8 seconds. This value can then be incremented every 8 seconds. This is especially useful for prolonged periods of parked time to avoid discharging the battery.

Another benefit of having RAM available is that it allows for self test implementation, where the last working configuration of the MC33903/4/5 can be saved. A typical use case is when a microcontroller stores known code in RAM as self test code. The microcontroller may then stop refreshing the watchdog and the SBC generates a $\overline{\text{RST}}$. After the reset, the microcontroller can then read the code that was stored in RAM and acknowledge that it is a self test operation.

Table 28. Internal memory registers A, B, C, and D, RAM_A, RAM_B, RAM_C, and RAM_D

MOSI First Byte [15-8] [b_15 b_14] 0_0xxx [P/N]	MOSI Second Byte, bits 7-0							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01 00 _ 001 P	Ram a7	Ram a6	Ram a5	Ram a4	Ram a3	Ram a2	Ram a1	Ram a0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 010 P	Ram b7	Ram b6	Ram b5	Ram b4	Ram b3	Ram b2	Ram b1	Ram b0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 011 P	Ram c7	Ram c6	Ram c5	Ram c4	Ram c3	Ram c2	Ram c1	Ram c0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 100 P	Ram d7	Ram d6	Ram d5	Ram d4	Ram d3	Ram d2	Ram d1	Ram d0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

5.6.7 CAN configuration

The CAN transceiver of the MC33903/4/5 family of SBCs includes three different modes of operation that can be configured via SPI in the CAN Register shown on Table 29. When the SBC transitions into Normal mode for the first time, the CAN transceiver will be in sleep mode with wake-up enabled. Any other transition into Normal after this one, the CAN state is user defined via bits b7 and b6 of the CAN Register. The Transmit and Receive mode can only be entered when the TxD is recessive and the 5V-CAN supply voltage is within specification. The 5V-CAN regulator must be enabled in the REG Register before going into Transmit and Receive mode. Once in Transmit and Receive mode, both the CAN driver and the receiver are enabled, the CAN bus lines are controlled by TxD and the CAN bus state is reported on RxD. Bits b5 and b4 determine the slew rate for the CAN bus lines dependent on module requirements. Bit b0 allows the microcontroller to select an $\overline{\text{INT}}$ trigger in the event of a fully defined CAN fault or as soon as the failure is detected. Refer to the datasheet for further CAN bus fault diagnostic information

Table 29. CAN register

MOSI First byte [15-8] [b_15 b_14] 10_000 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 000P	CAN mod[1]	CAN mod[0]	Slew[1]	Slew[0]	Wake-up 1/3	-	-	CAN int
Default state	1	0	0	0	0	-	-	0
Condition for default	note		POR		POR			POR

Bits	Description
b7 b6	**CAN mod[1], CAN mod[0]** - CAN interface mode control, Wake-up enable / disable
00	CAN interface in Sleep mode, CAN Wake-up disable.
01	CAN interface in receive only mode, CAN driver disable.
10	CAN interface is in Sleep mode, CAN Wake-up enable. In device LP mode, CAN Wake-up is reported by device Wake-up. In device Normal mode, CAN Wake-up reported by INT.
11	CAN interface in transmit and receive mode.
b5 b4	**Slew[1] Slew[0]** - CAN driver slew rate selection
00/11	FAST
01	MEDIUM
10	SLOW
b3	**Wake-up 1/3** - Selection of CAN Wake-up mechanism
0	3 dominant pulses Wake-up mechanism
1	Single dominant pulse Wake-up mechanism
b0	**CAN INT -** Select the CAN failure detection reporting
0	Select INT generation when a bus failure is fully identified and decoded (i.e. after 5 dominant pulses on TxCAN)
1	Select INT generation as soon as a bus failure is detected, event if not fully identified

Another operation of the CAN transceiver is the Receive only mode. When the CAN transitions into this mode, the CAN driver is disabled so any signal on the TxD will have no effect on the CAN bus lines. The CAN receiver stays enabled and the SPLIT pin is biased to 2.5 V so anything on the CAN bus lines will be reported on RxD. Note that the 5V-CAN regulator must be enabled for the CAN to properly operate in Receive only mode.

The CAN's sleep mode is the lowest current consumption mode. There are two options to place the CAN into Sleep mode: one is with wake-up capability and the second one is without it. For both Sleep modes, the CAN bus lines are disabled and terminated to GND via Rin (typically 25KΩ shown in Figure 54) and the SPLIT pin is high-impedance. When the wake-up is disabled, the only way for the CAN interface to transition out of Sleep mode is by the microcontroller via SPI command.

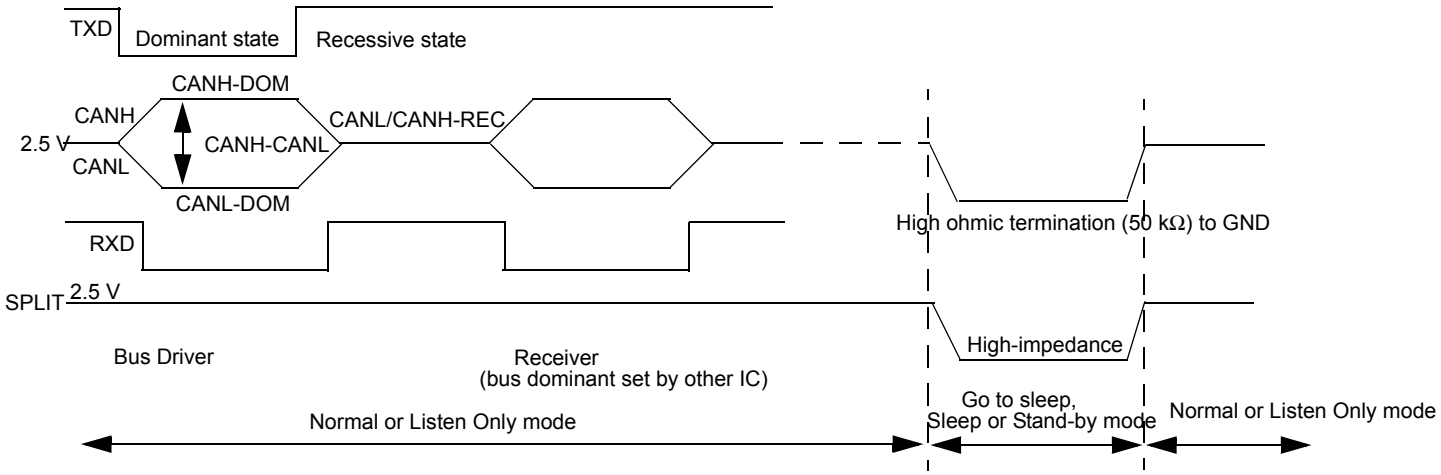
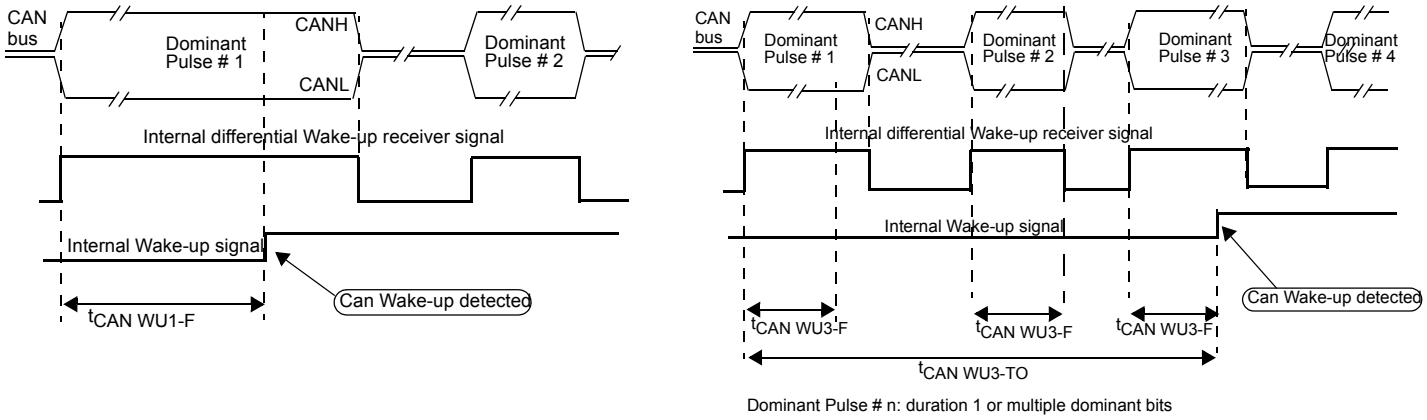


Figure 76. Bus signal in transmit/receive and low power mode

If the wake-up is enabled, the CAN bus lines are monitored for single or three-pulse wake-ups (dependent on bit b3 of the CAN Register). See Figure 77 for more details. In the event of a CAN bus wake-up, an $\overline{\text{INT}}$ is triggered to notify the microcontroller and the CAN wake-up flag is set. If the SBC (not just the CAN) was in Low Power mode, the CAN wake-up event will take the SBC out of Low Power mode.



Single Dominant Pulse Wake-Up

Pattern Wake-up - Multiple Dominant Detection

Figure 77. Single and three pulse wake-up

5.6.8 LIN configuration

The LIN transceiver of the MC33903/4/5 family of SBCs includes two different modes of operation that can be configured via SPI bits b7 and b6 in the LIN/1 and LIN2 Registers shown on Table 30 and Table 31. The LIN interface is able to transition into Transmit and Receive mode only when the TxD is in recessive state. If the microcontroller attempts to place the LIN interface in transmit and receive mode while the TxD is dominant, the SPI command is ignored and the LIN interface remains disabled. Also note that the 5V-CAN must be enabled for the LIN transceiver to be able to properly function in Transmit and Receive mode. Once in Transmit and Receive mode, both the LIN driver and the receiver are enabled, the LIN bus is controlled by TxD and the LIN bus state is reported on RxD. Bits b5 and b4 determine the slew rate for the LIN bus. To meet the LIN 2.1 protocol specification, the 20 kbit/s baud rate must be selected. To meet the J2602-2 LIN protocol specification, the 10 kbit/s baud rate must be selected. There is also a 'Fast' baud rate available for which the slew rate and timing is much faster than both of the LIN protocol specifications.

Table 30. LIN/1 register

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 10_ 011P	LIN mode[1]	LIN mode[0]	Slew rate[1]	Slew rate[0]	-	LIN T/1 on	-	V_{SUP} ext
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	**Description**
b7 b6	LIN mode [1], LIN mode [0] - LIN/1 interface mode control, Wake-up enable / disable
00	LIN/1 disable, Wake-up capability disable
01	not used
10	LIN/1 disable, Wake-up capability enable
11	LIN/1 Transmit Receive mode
b5 b4	Slew rate[1], Slew rate[0] LIN/1 slew rate selection
00	Slew rate for 20 kbit/s baud rate

Bits	Description
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b2	LIN T/1 on
0	LIN/1 termination OFF
1	LIN/1 termination ON
b0	V_{SUP} ext
0	LIN goes recessive when device $V_{SUP/2}$ is below typically 6.0 V. This is to meet J2602 specification
1	LIN continues operation below $V_{SUP/2}$ 6.0 V, until 5 V-CAN is disabled.

Bit b2 allows the microcontroller to enable or disable the LIN-T1 or LIN-T2 LIN termination when in Transmit and Receive mode. Note that these must have been initialized as LIN terminations in the INIT LIN I/O Register (see Table 15). Bit b0 allows for the continuous operation of the LIN interface when Vsup/2 drops below typically 6.0 V and until the 5V-CAN is disabled. Note that the J2602-2 LIN specification requires that the LIN interface be recessive if the V_{SUP2} voltage is below typically 6.0 V.

Table 31. LIN2 Register

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 100P	LIN mode[1]	LIN mode[0]	Slew rate[1]	Slew rate[0]	-	LIN T2 on	-	V_{SUP} ext
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	Description
b7 b6	LIN mode [1], LIN mode [0] - LIN 2 interface mode control, Wake-up enable / disable
00	LIN2 disable, Wake-up capability disable
01	not used
10	LIN2 disable, Wake-up capability enable
11	LIN2 Transmit Receive mode
b5 b4	Slew rate[1], Slew rate[0] LIN 2slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b2	LIN T2 on
0	LIN 2 termination OFF

Bits	Description
1	LIN 2 termination ON
b0	V_{SUP} ext
0	LIN goes recessive when device $V_{SUP/2}$ is below typically 6.0 V. This is to meet J2602 specification
1	LIN continues operation below $V_{SUP/2}$ 6.0 V, until 5 V-CAN is disabled.

The LIN's sleep mode is the lowest current consumption mode. There are two options to place the LIN into Sleep mode: one is with wake-up capability and the second one is without it. For both sleep modes, the LIN bus driver is disabled and internally pulled up to V_{SUP2} via a typically 725 kΩ resistor. This allows for ultra low current consumption (typically 3.0 µA) due to the LIN interface. When the wake-up is disabled, the only way for the LIN to transition out of sleep mode is by the microcontroller via a SPI command.

If the wake-up is enabled, the LIN bus is monitored for a wake-up pulse. In the event of a LIN bus wake-up, an $\overline{INT}$ is triggered to notify the microcontroller and the LIN wake-up flag is set.

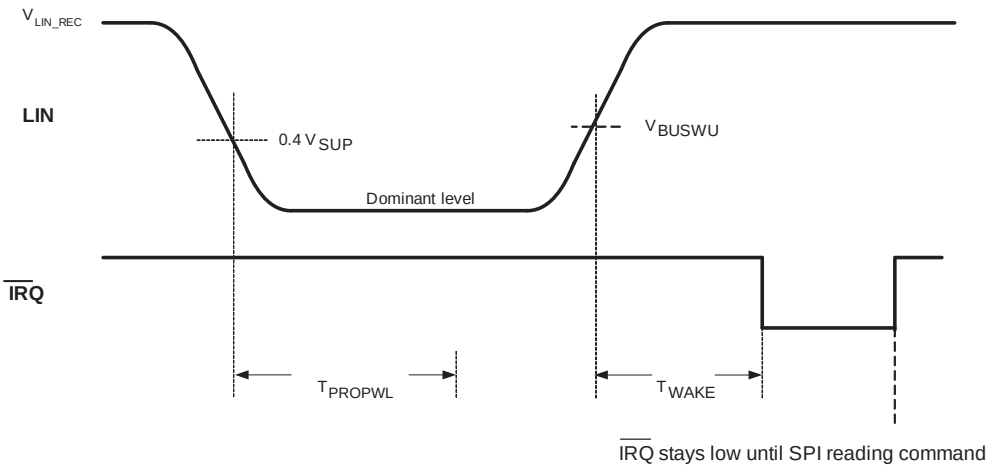


Figure 78. LIN wake-up LP V_{DD} on mode timing

If the SBC (not just the LIN) was in Low Power VDD ON mode, the LIN wake-up event will take the SBC out of Low Power mode. See Figure 78. If the SBC (not just the LIN) was in Low Power VDD OFF mode, the LIN wake-up event will take the SBC out of Low Power mode. See Figure 79.

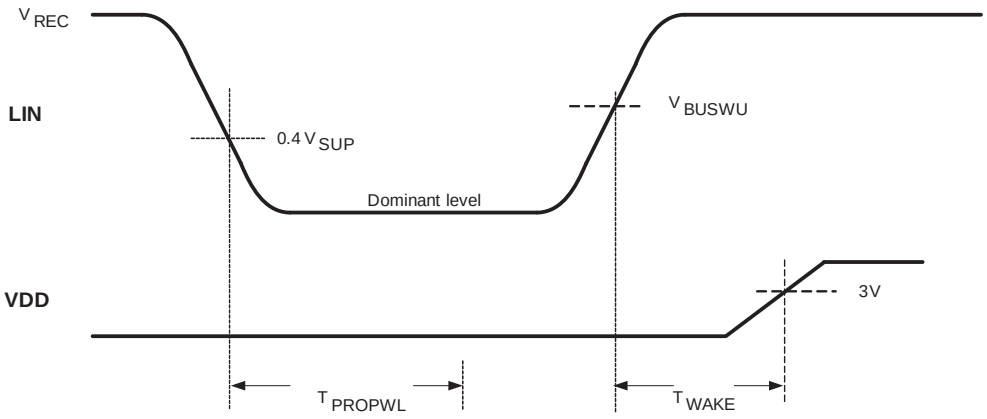


Figure 79. LIN wake-up V_{DD} off mode timing

See Table 32 for more details on LIN interface behavior due to failures.

Table 32. LIN faults

FAULT	FUNCTIONNAL MODE	CONDITION	CONSEQUENCE	RECOVERY
LIN supply undervoltage	TXD RXD	LIN supply voltage < 6.0 V (typically)	LIN transmitter in recessive State	Condition gone
TXD Pin Permanent Dominant		TXD pin low for more than t_{TXDDOM}	LIN transmitter in recessive State	Condition gone
LIN Thermal Shutdown	TXD RXD	LIN driver temperature > 160 °C (typically)	LIN transmitter and receiver disabled HS turned off	Condition gone

5.7 Low power modes

There are two low power modes available for the MC33903/4/5 family of SBCs. The Low Power VDD OFF mode is the lowest current consumption mode available where the SBC will consume a typical of 15 µA. In this case, the V_{DD} is disabled so the microcontroller is unpowered. The Low power VDD ON mode allows the microcontroller to stay enabled, but with very limited current capability. During Low Power VDD ON mode, the SBC's current draw is typically 25 µA.

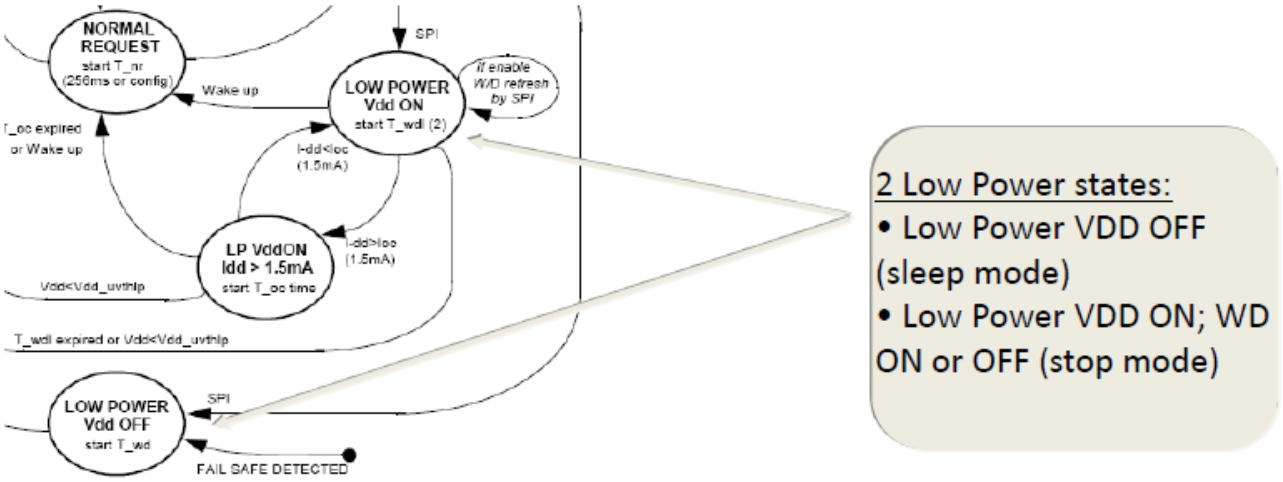


Figure 80. Low power states diagram

5.7.1 Low power VDD OFF

Low Power VDD OFF mode can be entered via the MODE Register shown in Table 33 with the option to enable or disable the Forced Wake-up timer and the Cyclic Sense functionality (see Figure 84 for more details) dependent on bits b7, b6, b5, b4, and b3.

Table 33. MODE register

MOSI First Byte [15-8] [b_15 b_14] 01_110 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 110 P	mode[4]	mode[3]	mode[2]	mode[1]	mode[0]	Rnd_b[2]	Rnd_b[1]	Rnd_b[0]
Default state	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 1. LP V_{DD} OFF selection and FWU/cyclic sense selection

b7, b6, b5, b4, b3	FWU	Cyclic Sense
0 1100	OFF	OFF
0 1101	OFF	ON
0 1110	ON	OFF
0 1111	ON	ON

When transitioning into Low Power VDD OFF mode, the Vaux and the 5V-CAN are disabled and the $\overline{RST}$ and $\overline{INT}$ are asserted 'low'. The SBC monitors for external wake-up events during Low Power VDD OFF mode. The wake-up events available during this mode are: CAN, LIN, I/O, and Forced Wake-up (refer to Figure 81).

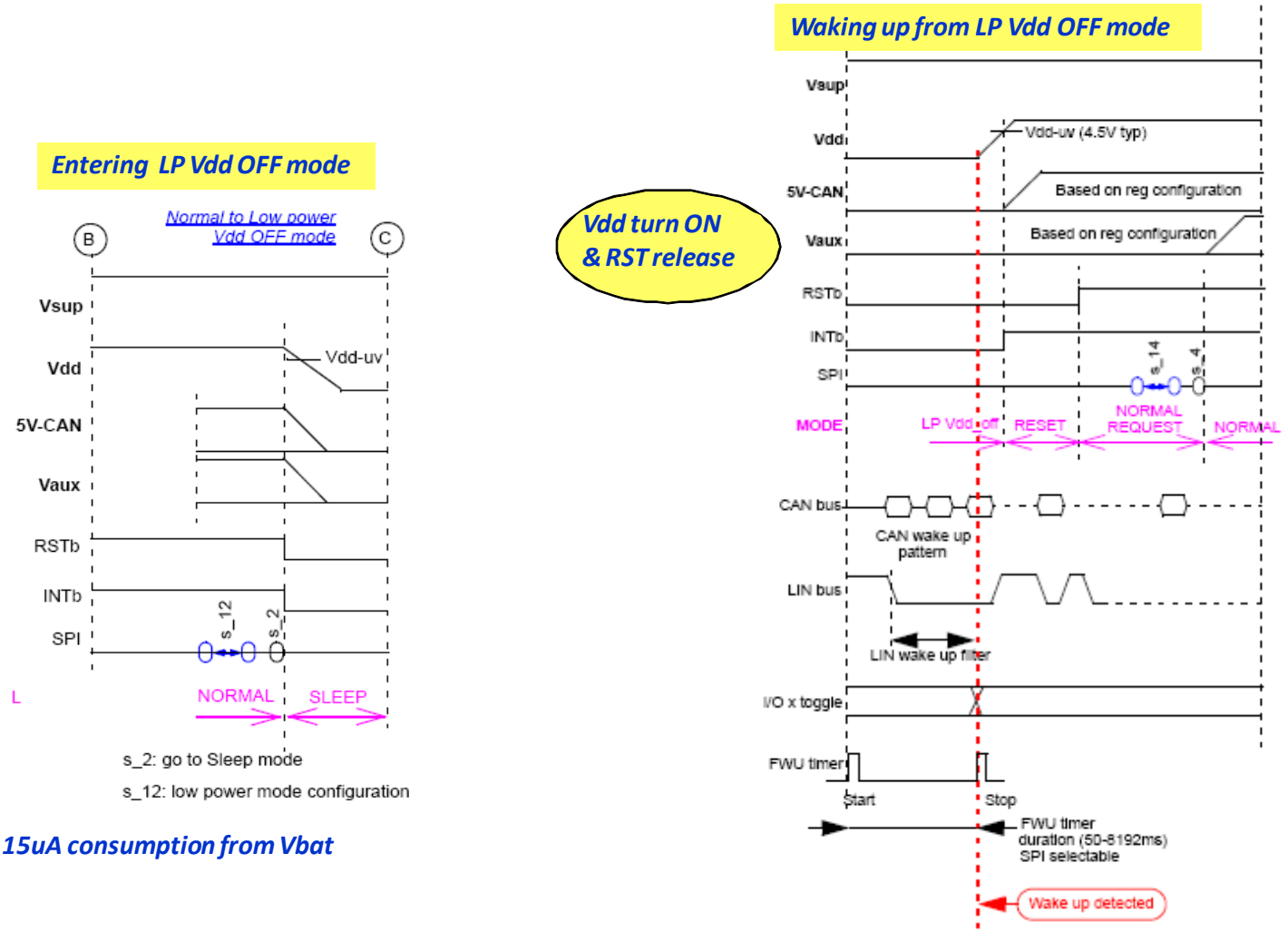


Figure 81. Transitioning into and out of low power VDD off mode

When a wake-up is detected, the VDD regulator starts to ramp up. When the voltage reaches the VDD undervoltage threshold (typ. 4.5), $\overline{INT}$ is de-asserted and the SBC transitions into RESET mode (see Figure 81). $\overline{RST}$ will remain 'low' for 1.0 ms, 5.0 ms, 10 ms, or 20 ms dependent on initialized value of bits b4 and b3 of the INIT REG Register (Refer to Table 13). Once the $\overline{RST}$ is de-asserted, the SBC transitions into Normal Request mode where the 256 ms or configured timer will start. A valid watchdog refresh is then needed to transition into Normal mode. See Figure 82.

The wake-up sources are reported to the SPI registers (see Table 12).

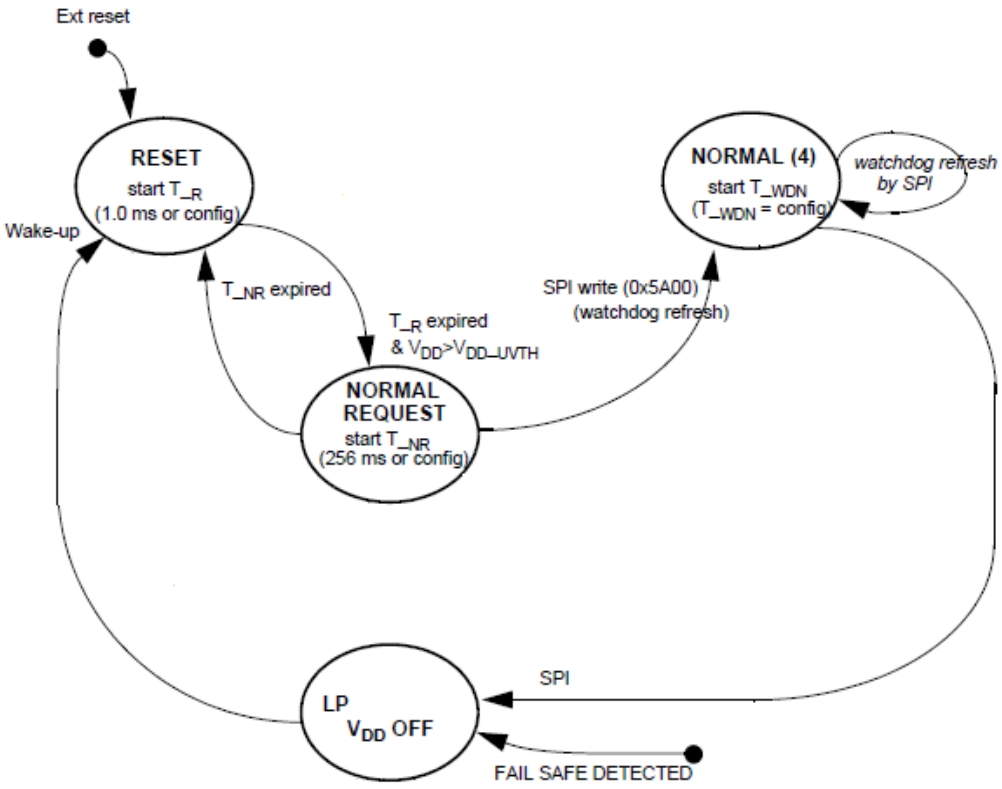
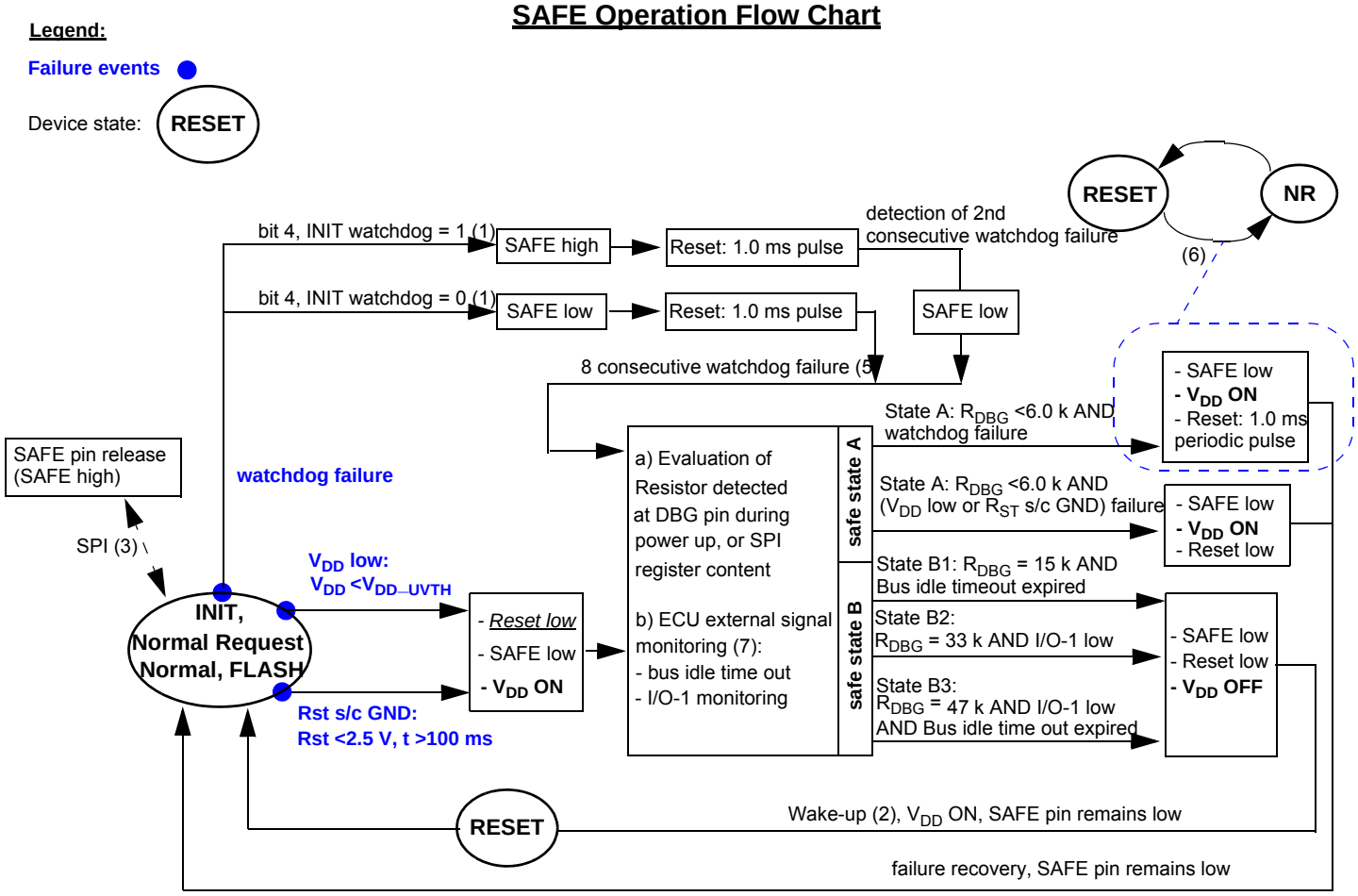


Figure 82. Normal, low power VDD off, reset, and normal request state diagram

The SBC can also automatically enter Low Power VDD OFF mode in the event of a fail SAFE condition dependent on the DBG pin resistor value configuration (see Figure 83).

SAFE Operation Flow Chart



1) bit 4 of INIT Watchdog register
2) Wake-up event: CAN, LIN or I/O-1 high level (if I/O-1 Wake-up previously enabled)
3) SPI commands: 0xDD00 or 0xDD80 to release SAFE pin
4) Recovery: reset low condition released, V_{DD} low condition released, correct SPI watchdog refresh
5) detection of 8 consecutive watchdog failures: no correct SPI watchdog refresh command occurred for duration of 8 x 256 ms.
6) Dynamic behavior: 1.0 ms reset pulse every 256 ms, due to no watchdog refresh SPI command, and device state transition between RESET and NORMAL REQUEST mode, or INIT RESET and INIT modes.
7) 8 second timer for bus idle timeout. I/O-1 high to low transition.

Figure 83. FSAFE operation flow chart

When the cyclic sense functionality is selected during Low Power VDD ON or OFF mode, the SBC will periodically pulse I/O-0 to monitor any state transitions on the rest of the I/Os. Cyclic sense is primarily designed to decrease current consumption and optimized for closed contact switch applications as shown in Figure 84. During Normal mode, when the current consumption is not as critical, I/O-0 functions as a pull-up to VSUP2 for the rest of the I/Os. By implementing the cyclic sense feature, when the SBC transitions into Low Power VDD ON or OFF mode, there is no current flow in the I/Os since I/O-0 is also grounded. The SBC will then pulse I/O-0 and monitor the state of the rest of the I/Os every cyclic sense period (as configured in Timer Register B [see Table 19]). The pulse width duration is selected during the initialization phase of the SBC dependent on bits b1 and b0 of the Initialization Regulator register (refer to Table 13).

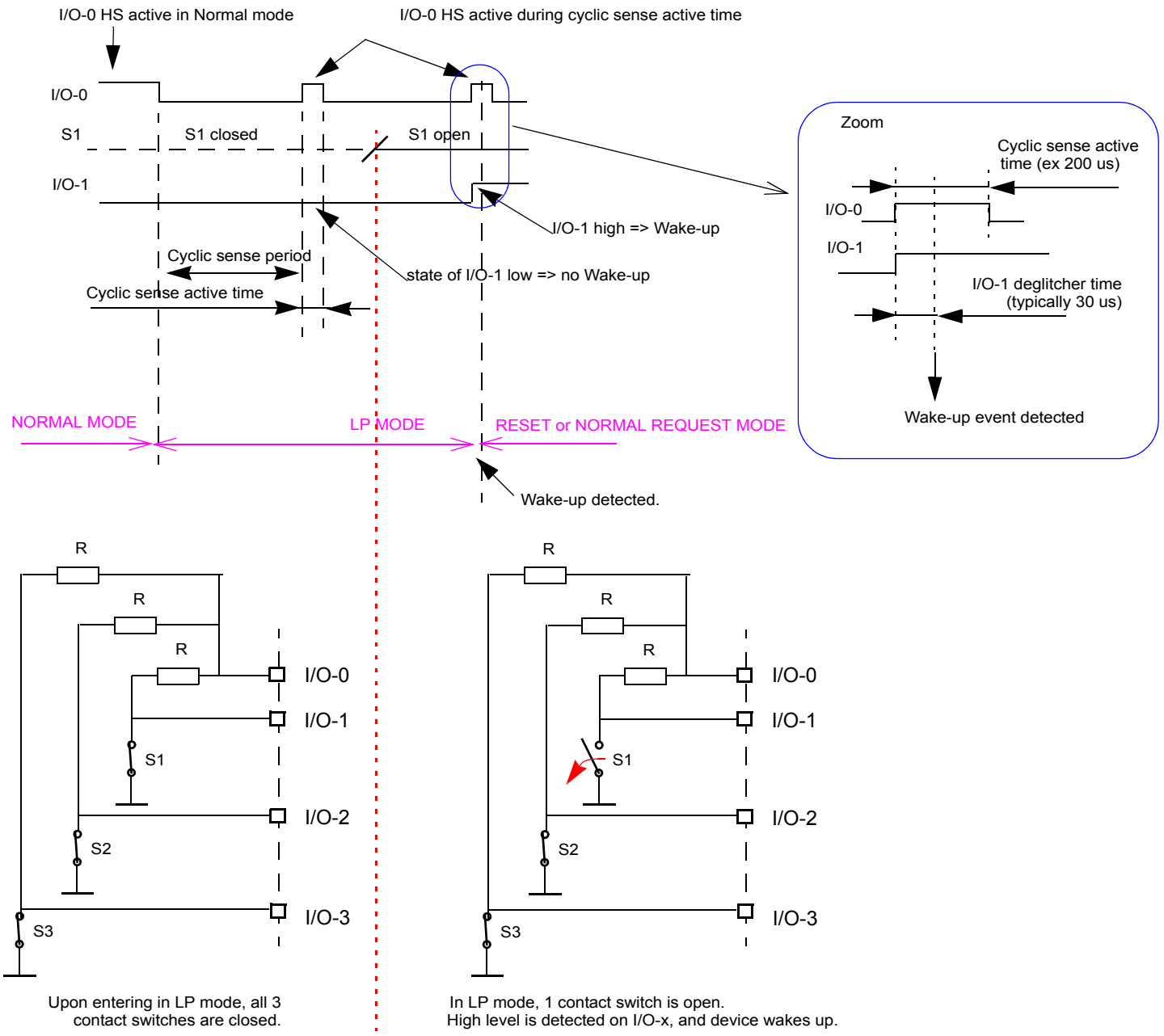


Figure 84. Cyclic sense operation - switch to GND, wake-up by open switch

5.7.2 Low power VDD on

Low Power VDD ON mode can be entered via the MODE Register shown in Table 34 with the option to enable or disable the Forced Wake-up timer, Cyclic Sense, Cyclic Interrupt (refer to Figure 87), and Watchdog operation dependent on bits b7, b6, b5, b4, and b3.

Table 34. MODE register, mode

MOSI First Byte [15-8] [b_15 b_14] 01_110 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 110 P	mode[4]	mode[3]	mode[2]	mode[1]	mode[0]	Rnd_b[2]	Rnd_b[1]	Rnd_b[0]
Default state	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 2. LP VDD on selection and operation mode

b7, b6, b5, b4, b3	FWU	Cyclic Sense	Cyclic INT	Watchdog
1 0000	OFF	OFF	OFF	OFF
1 0001	OFF	OFF	OFF	ON
1 0010	OFF	OFF	ON	OFF
1 0011	OFF	OFF	ON	ON
1 0100	OFF	ON	OFF	OFF
1 0101	OFF	ON	OFF	ON
1 0110	OFF	ON	ON	OFF
1 0111	OFF	ON	ON	ON
1 1000	ON	OFF	OFF	OFF
1 1001	ON	OFF	OFF	ON
1 1010	ON	OFF	ON	OFF
1 1011	ON	OFF	ON	ON
1 1100	ON	ON	OFF	OFF
1 1101	ON	ON	OFF	ON
1 1110	ON	ON	ON	OFF
1 1111	ON	ON	ON	ON
b2, b1, b0	Random Code inverted, these 3bits are the inverted bits obtained from the previous SPI command. The usage of these bits are optional and must be previously selected in the INIT MISC register [See bit 7 (LPM w RNDM) in Table 16]			

When transitioning into Low Power VDD ON mode, the Vaux and the 5V-CAN are disabled and the $\overline{RST}$ and $\overline{INT}$ remain 'high' (Refer to Figure 85). The SBC will monitor for all the same wake-ups as in Low Power VDD OFF mode (CAN, LIN, I/O, and Forced Wake Up). Additionally, the SBC will monitor for a dedicated SPI command (0x5C10) which allows the transition from Low Power VDD ON to Normal Request mode. During Low Power VDD ON mode, the SBC will also monitor for current consumption on the VDD regulator that exceeds a minimum of 1.0 mA for longer than a configurable amount of time dependent on bits b7, b6, and b5 in Timer Register A (refer to Table 18).

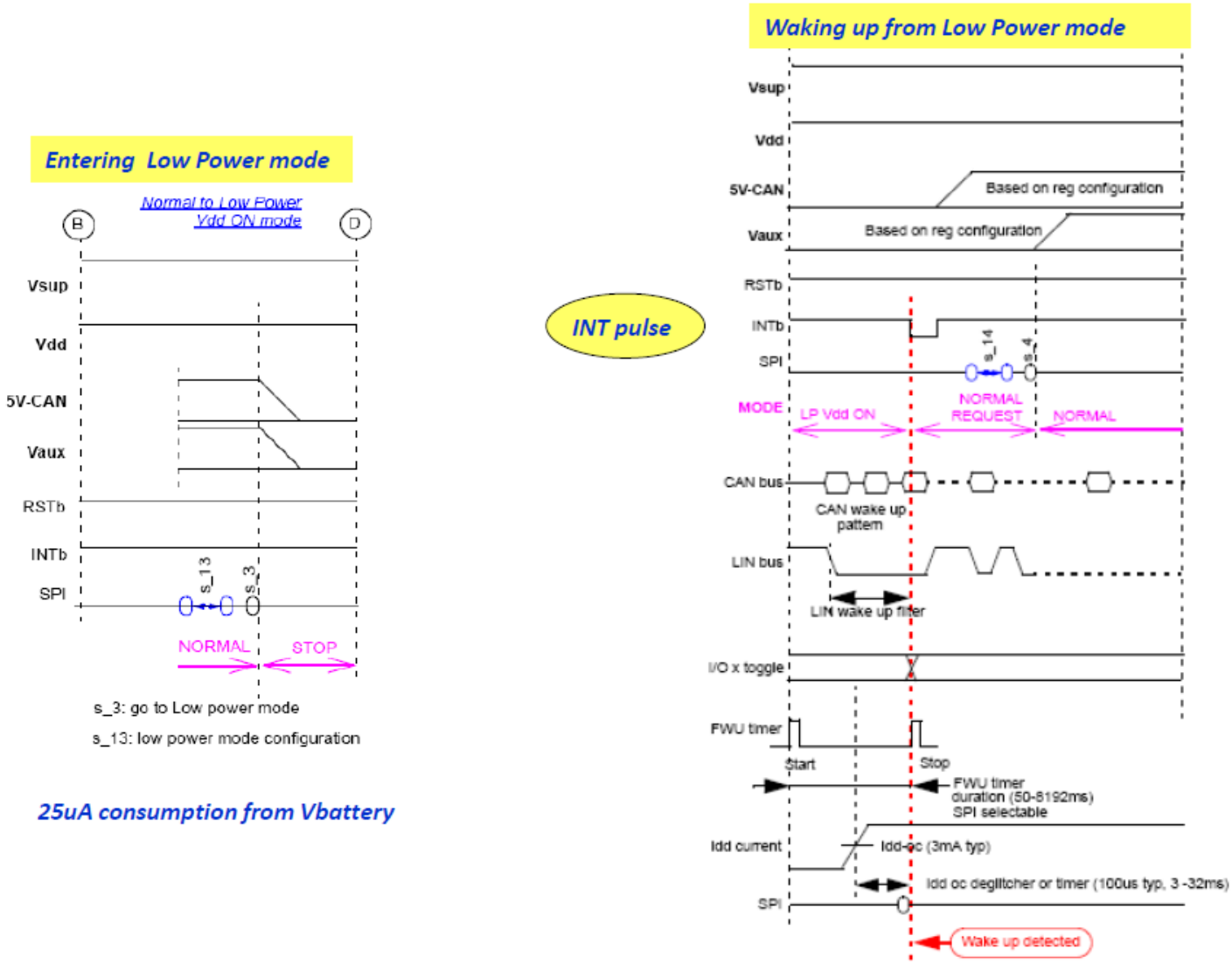


Figure 85. Transitioning into and out of low power VDD on mode

When a wake-up is detected, the $\overline{\text{INT}}$ is asserted 'low' to notify the microcontroller and the SBC transitions into Normal Request mode. When the $\overline{\text{INT}}$ is de-asserted, the 5V-CAN voltage regulator may start to ramp up dependent on configuration. The microcontroller must then send a dedicated SPI command (0x5C10) to transition into Normal Request mode where the 256ms or configured timer will start. A valid watchdog refresh is then needed to transition into Normal mode. See Figure 86.

The Wake-up sources are reported to the SPI registers (see Table 12).

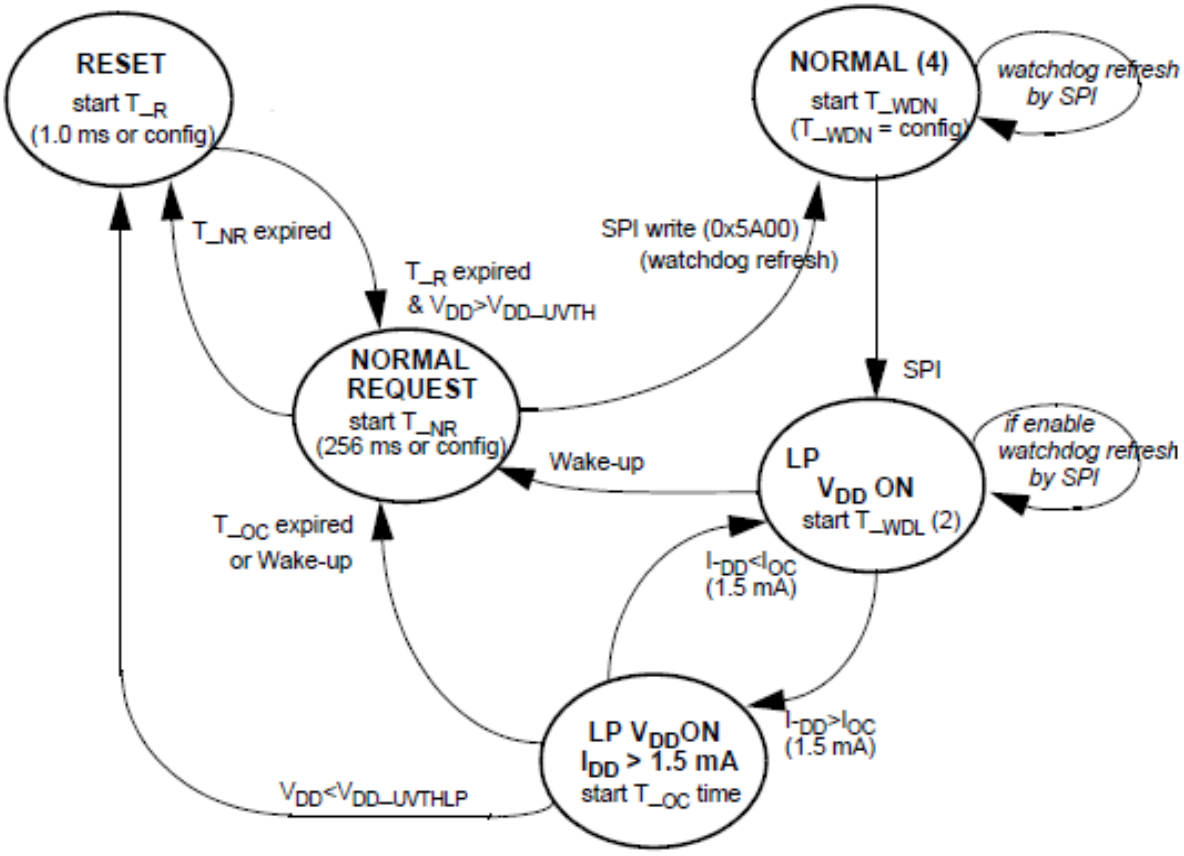


Figure 86. Normal, low power VDD on, reset, and normal request state diagram

When the cyclic Interrupt functionality is selected for Low Power VDD ON, the SBC will periodically interrupt the microcontroller. Upon the reception of the interrupt, the microcontroller must then acknowledge the Interrupt by reading back the 'device control bits' of the **Watchdog Refresh** address in the Device Registers by sending 0x1B00 = 00**01 101**1 0000 0000 (address is in **bold**). Refer to Table 35 and Table 36. The microcontroller must then invert the random bits b7 - b0 read and send back to the SBC with a watchdog refresh write SPI command (0x5AXX) within the cyclic interrupt period. To exit Low Power VDD ON mode, the microcontroller must send the dedicated 0x5C10 SPI command within the cyclic interrupt period. When no SPI command or an improper SPI command is sent, the SBC will cease cyclic interrupt operation and exit out of Low Power VDD ON mode by asserting $\overline{RST}$. The SBC then transitions into Normal Request Mode. Refer to Figure 87.

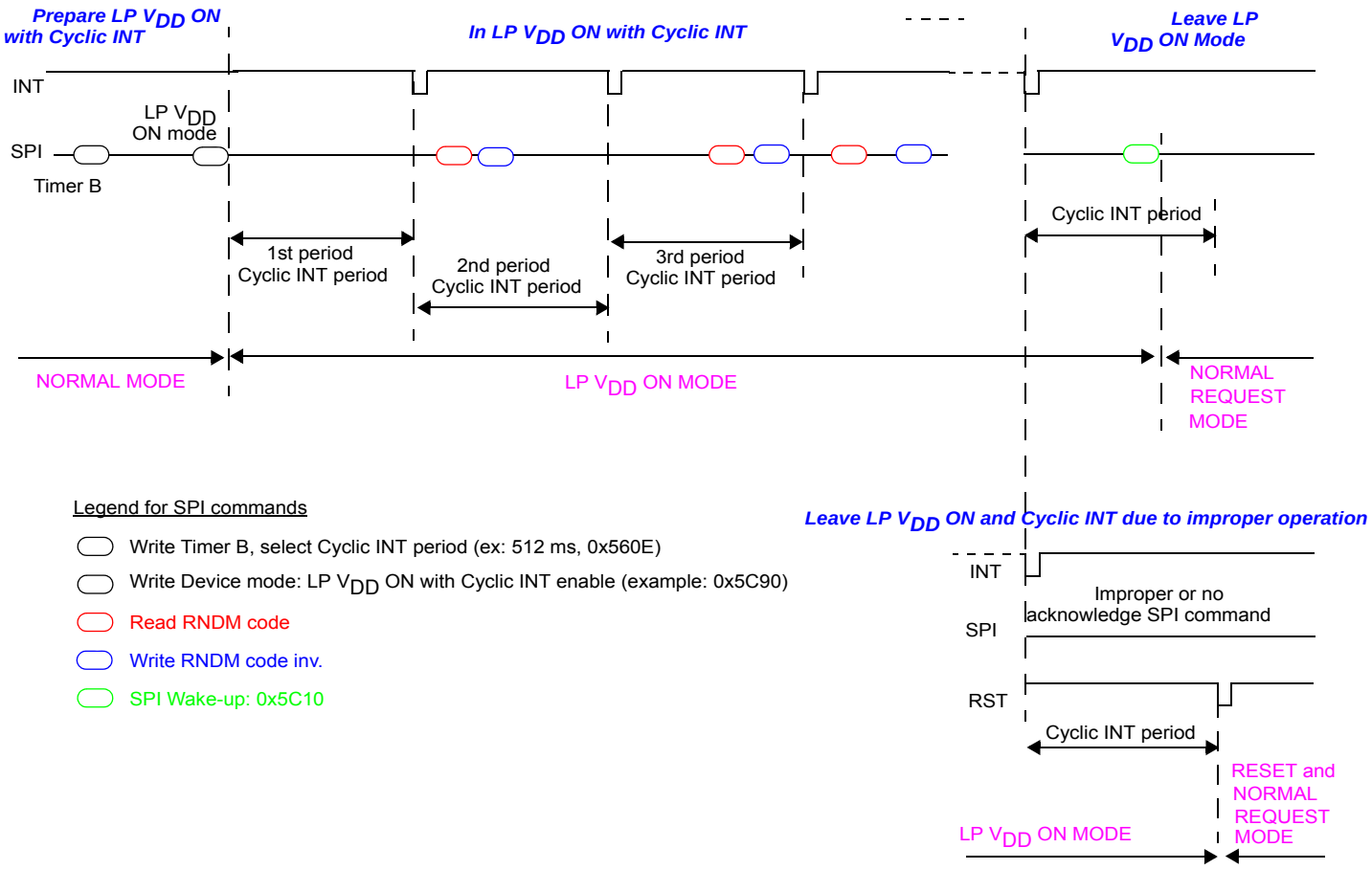


Figure 87. Cyclic interrupt operation

During Low Power VDD ON mode, the SBC is able to maintain the microcontroller enabled by supplying the required voltage at limited current capability. The SBC is able to tolerate an increase in current consumption above a minimum of 1.0 mA from the microcontroller for as long as 32 ms and as short as 3.0 ms (default) dependent on bits b7, b6, and b5 configuration in the Timer Register A (refer toTable 18) without waking up. This reduces the module's total current consumption by reducing the number of multiple Interrupts as shown in Figure 88.

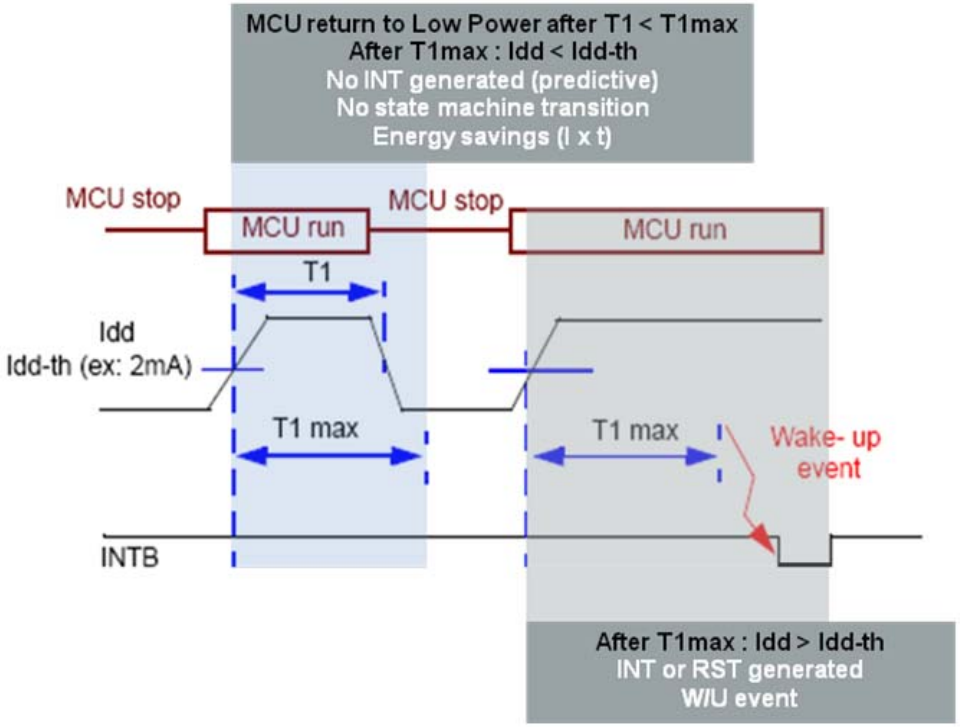


Figure 88. Low power VDD on current monitoring

5.8 Secured SPI

The MC33903/4/5 family of SBCs allows the transition to special modes by means of secured SPI. These special modes are the Initialization, Flash, and Reset modes. To transition into these states from Normal mode, Secured SPI is required because for safety reasons it is critical not to transition into these states by accident. Figure 89 shows an example of how Secured SPI works in a transition from Normal to Initialization mode.

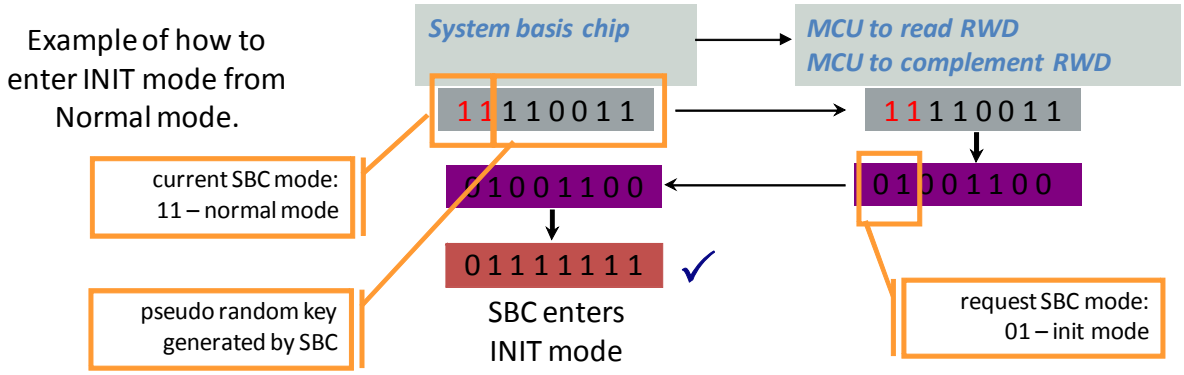


Figure 89. Secured SPI operation

To transition into Initialization, Flash, or Reset mode from Normal mode, the microcontroller has to read back the 'device control bits' of the **Specific Modes** address in the Device Registers by sending 0x1300 = 00**01 001**1 0000 0000 (address is in **bold**). Refer to Table 35 and Table 36. The microcontroller must then invert the random bits b5 - b0 read and set bits b7 and b6 according to desired mode for the SBC to transition into (refer to Table 37). The SBC will then verify that all random bits were properly complemented and transition into the specified mode.

Table 35. SPI capabilities with options

Type of Command	MOSI/MISO	Control bits [15-14]	Address [13-9]	Parity/Next bits [8]	Bit 7	Bits [6-0]
Read back of “device control bits” (MOSI bit 7 = 0) OR Read specific device information (MOSI bit 7 = 1)	MOSI	00	address	1	0	000 0000
	MISO	Device Fixed Status (8 bits)			Register control bits content	
	MOSI	00	address	1	1	000 0000
	MISO	Device Fixed Status (8 bits)			Device ID and I/Os state	
Write device control bit to address selected by bits (13-9). MISO return 16 bits device status	MOSI	01	address	(note)	Control bits	
	MISO	Device Fixed Status (8 bits)			Device Extended Status (8 bits)	
Reserved	MOSI	10	Reserved			
	MISO	Reserved				
Read device flags and Wake-up flags, from register address (bit 13-9), and sub address (bit 7). MISO return fixed device status (bit 15-8) + flags from the selected address and sub-address.	MISO	11	address	Reserved	0	Read of device flags form a register address, and sub address LOW (bit 7)
	MOSI	Device Fixed Status (8 bits)			Flags	
	MISO	11	address	1	1	Read of device flags form a register address, and sub address HIGH (bit 7)
	MOSI	Device Fixed Status (8 bits)			Flags	

Table 36. Device registers with corresponding address

Address MOSI[13-9] A4...A0	Description	Quick Ref. Name	Functionality
0_0000	Analog Multiplexer	MUX	1) Write “device control bits” to register address. 2) Read back register “control bits”
0_0001	Memory byte A	RAM_A	1) Write “data byte” to register address. 2) Read back “data byte” from register address
0_0010	Memory byte B	RAM_B	
0_0011	Memory byte C	RAM_C	
0_0100	Memory byte D	RAM_D	
0_0101	Initialization Regulators	Init REG	1) Write “device initialization control bits” to register address. 2) Read back “initialization control bits” from register address
0_0110	Initialization Watchdog	Init watchdog	
0_0111	Initialization LIN and I/O	Init LIN I/O	
0_1000	Initialization Miscellaneous functions	Init MISC	
0_1001	Specific modes	SPE_MODE	1) Write to register to select device Specific mode, using “Inverted Random Code”. 2) Read “Random Code”
0_1010	Timer_A: watchdog & LP MCU consumption	TIM_A	1) Write “timing values” to register address. 2) Read back register “timing values”
0_1011	Timer_B: Cyclic Sense & Cyclic Interrupt	TIM_B	
0_1100	Timer_C: watchdog LP & Forced Wake-up	TIM_C	
0_1101	Watchdog Refresh	watchdog	Watchdog Refresh Commands

Table 36. Device registers with corresponding address

Address MOSI[13-9] A4...A0	Description	Quick Ref. Name	Functionality
0_1110	Mode register	MODE	1) Write to register to select LP mode, with optional “Inverted Random code” and select Wake-up functionality 2) Read operations: Read back device “Current mode” Read “Random Code”, Leave “Debug mode”
0_1111	Regulator Control	REG	1) Write “device control bits” to register address, to select device operation. 2) Read back register “control bits”. 3) Read device flags from each of the register addresses.
1_0000	CAN interface control	CAN	
1_0001	Input Output control	I/O	
1_0010	Interrupt Control	Interrupt	
1_0011	LIN1 interface control	LIN1	
1_0100	LIN2 interface control	LIN2	

Table 37. Specific Mode Register, SPE_MODE

MOSI First Byte [15-8] [b_15 b_14] 01_001 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 01_ 001 P	Sel_Mod[1]	Sel_Mod[0]	Rnd_C5b	Rnd_C4b	Rnd_C3b	Rnd_C2b	Rnd_C1b	Rnd_C0b
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	Description
b7, b6	**Sel_Mod[1], Sel_Mod[0]** - Mode selection: these 2 bits are used to select which mode the device will enter upon a SPI command.
00	RESET mode
01	INIT mode
10	FLASH mode
11	N/A
b5....b0	**[Rnd_C4b... Rnd_C0b]** - Random Code inverted, these six bits are the inverted bits obtained from the SPE MODE Register read command.

5.9 Normal request, reset, and flash modes

In addition to the Initialization mode described in Section Initializing the SBC, the MC33903/4/5 family of SBCs implements three other non-Normal functional modes that provide the module designer the flexibility to implement the SBC's feature set with configurable timings.

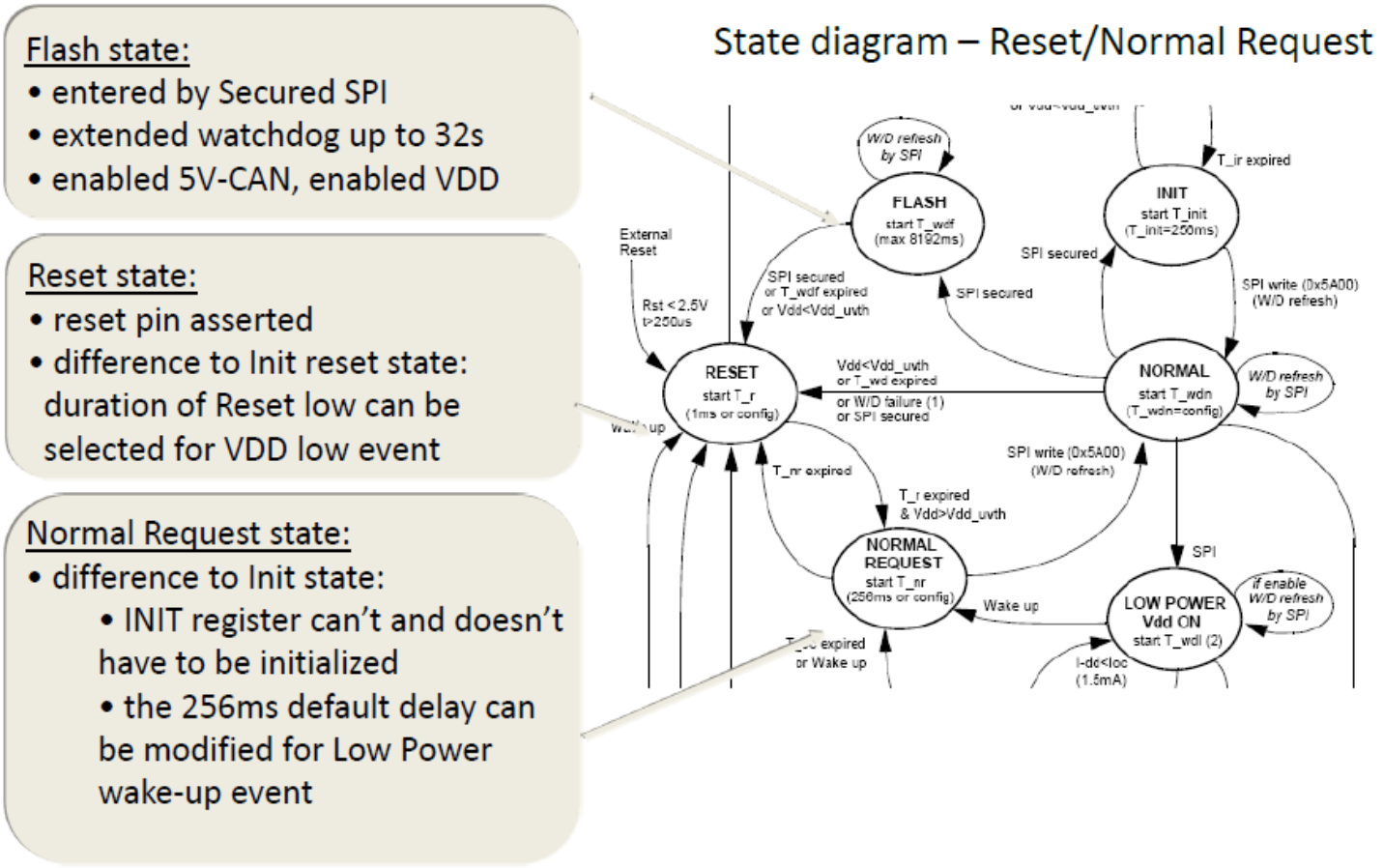


Figure 90. Normal request, reset and flash state diagram

Normal Request mode is automatically entered after a Reset or a wake-up event from Low Power VDD ON mode. When the SBC transitions into Normal Request from Reset mode, the 256 ms timer starts. Different durations can be configured by SPI when normal request is entered from Low Power VDD ON mode. A simple watchdog re-fresh SPI command (0x5A00) is then necessary to transition out of Normal Request into Normal mode. If the watchdog refresh SPI command does not occur within the 256 ms (or the shorter user defined time out), then the device will transition into Reset mode.

The SBC can also enter Reset from Normal mode, but only via Secured SPI. During Reset mode, the RST pin is asserted 'low' and the SBC can also transition into this state from Normal Request, Low Power VDD ON, and Flash mode when the watchdog is not triggered or if a VDD low condition is detected. The duration of reset is typically 1.0 ms by default. A longer reset pulse can be configured, but only when the Reset mode is entered from a VDD low condition. Reset pulse will always be 1.0 ms when Reset mode is entered due to wrong watchdog refresh command.

In Flash mode, the software watchdog period can be extended up to 32 seconds. This allows programming of the MCU flash memory while minimizing the software overhead to refresh the watchdog. The SBC can transition into and out of Flash mode by Secured SPI command. When transitioning out of Flash mode, the SBC will go into Reset mode. The SBC will also transition out of Flash into Reset mode due to an incorrect or missing watchdog refresh. Note that the advanced watchdog is not available in Flash mode. An interrupt can be generated at 50% of the watchdog period.

Note: CAN interface operates in Flash mode to allow flash via CAN bus, inside the vehicle.

6 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Document number and description		URL
33903/4/5	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC33903-MC33904-MC33905.pdf
NXP.com Support Pages		**URL**
MC33903 Product Summary Page		http://www.nxp.com/MC33903
MC33904 Product Summary Page		http://www.nxp.com/MC33904
MC33905 Product Summary Page		http://www.nxp.com/MC33905
Automotive Home Page		http://www.nxp.com/products/automotive-products:MC_50802
Analog Home Page		http://www.nxp.com/products/power-management:POWER-MANAGEMENT

7 Revision history

Revision	Date	Description
1.0	9/2013	• Initial release
2.0	7/2014	• Added description of the MUX register writing versus 5V-CAN behavior.
3.0	10/2016	• Updated document to NXP form and style • Added VSUP ramp up slew rate
4.0	6/2017	• Corrected typo in Figure 26 (changed 50 V/ms to 50 mV/ms)
5.0	12/2017	• Updated Watchdog operation

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12/2017