ES_FXLS8967AF_FXLS8974CF

Errata sheet for FXLS8967AF and FXLS8974CF

Rev. 1.1 — 18 April 2022 **Errata sheet**

Document information

Information	Content
Keywords	FXLS8967AF, FXLS8974CF
Abstract	This errata sheet describes the known functional problems and/or deviations from the product electrical specifications as of the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1.1	20220418	Corrected typo in document title replacing "FXLS8964AF" with "FXLS8967AF".
1	20220325	Initial release.

1 Product identification

The WHO_AM_I register (address 13h) identifies the device.

The PROD_REV register (address 12h) identifies the device revision.

This Errata sheet covers the following devices:

Table 1. Device identification table

Identifier	WHO_AM_I	PROD_REV	Device
A	87h	13h	FXLS8967AF
B	86h	14h	FXLS8974CF

2 Errata overview

Table 2. Functional problems table

Functional problems	Short description	Identifier	Detailed description
E1	Noise coupling in analog front end (AFE) measurements during serial communication	A, B	Section 3.1

3 Functional problems detail

3.1 E1: Communication noise

3.1.1 Introduction

This erratum is related to the noise coupling in sensor measurements when serial communications (through I^2C or SPI) overlap with the measurement phase of the device.

3.1.2 Problem

I^2C / SPI serial bus signals, associated to the sensor digital pins SA0 / SPI_MISO, SDA / SPI_MOSI / SPI_DATA and SCL / SCLK contain by nature many rising and falling transitions. Under very specific circumstances, further described in this errata sheet, there is a small risk that acceleration measurements are affected by this digital communication activity.

When serial bus Data and/or Clock signals toggle during the AFE measurement sequence, and only for a small fraction of the device population, those pins may couple noise into sensor's internal sensitive voltage node. This can affect the magnitude of the current measurements, causing sporadic spikes (see Figure 1, and Figure 2) also referred to as communication noise or glitches.

3.1.2.1 Measurement details for figures

Figure 1 through Figure 4 provide illustrations of the Errata with real measurements, performed under following conditions:

- Device settings: FSR = 4 g, ODR = 3200 Hz, LPM, horizontal position
- INT1 configuration: DRDY event, active Low, Push-Pull output
- SPI settings: 4-wire, 4 MHz Clock Frequency, V_{DD} = 3.3 V

- Data reading is either asynchronous, that is, done at a random time, or driven by the Data Ready Interrupt (DRDY event)
- Acceleration data are read one axis at a time, therefore there are 3 consecutive read transactions, 4 bytes each. Obviously this could be optimized doing a single 8 bytes transaction to collect XYZ data altogether.

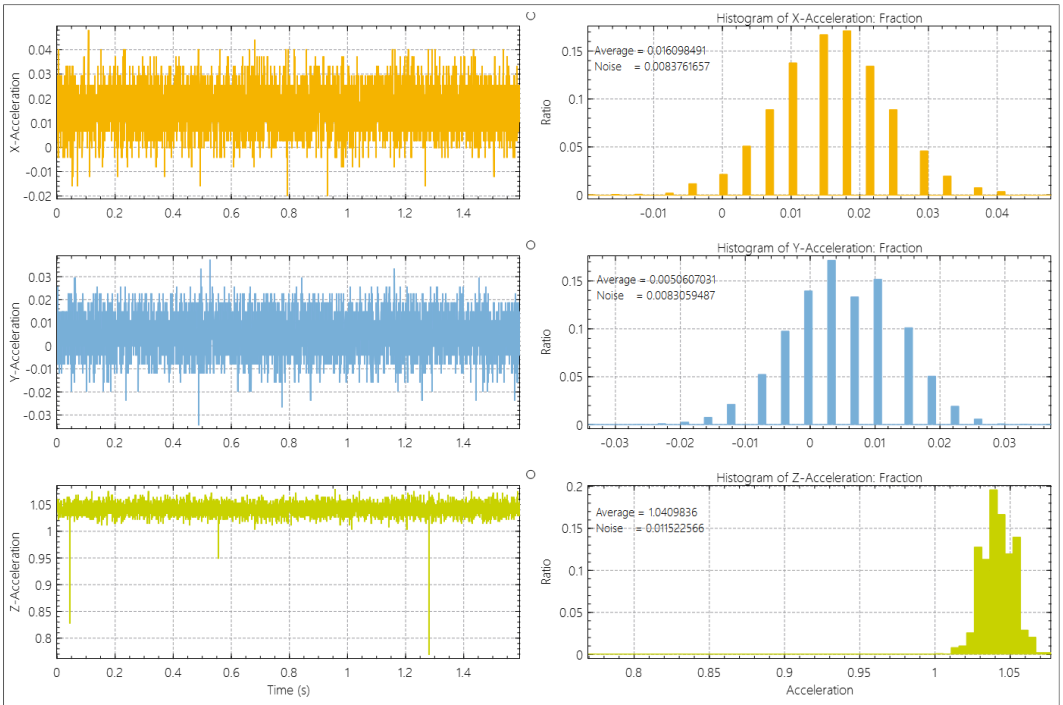

Figure 1. Acceleration data (in g): Plot vs Time and Histogram, asynchronous data reading

Note: *This data corruption is observed when measured acceleration is away from 0 g. As a result, the data corruption is only present on the Z axis in Figure 1 as the device is horizontal..*

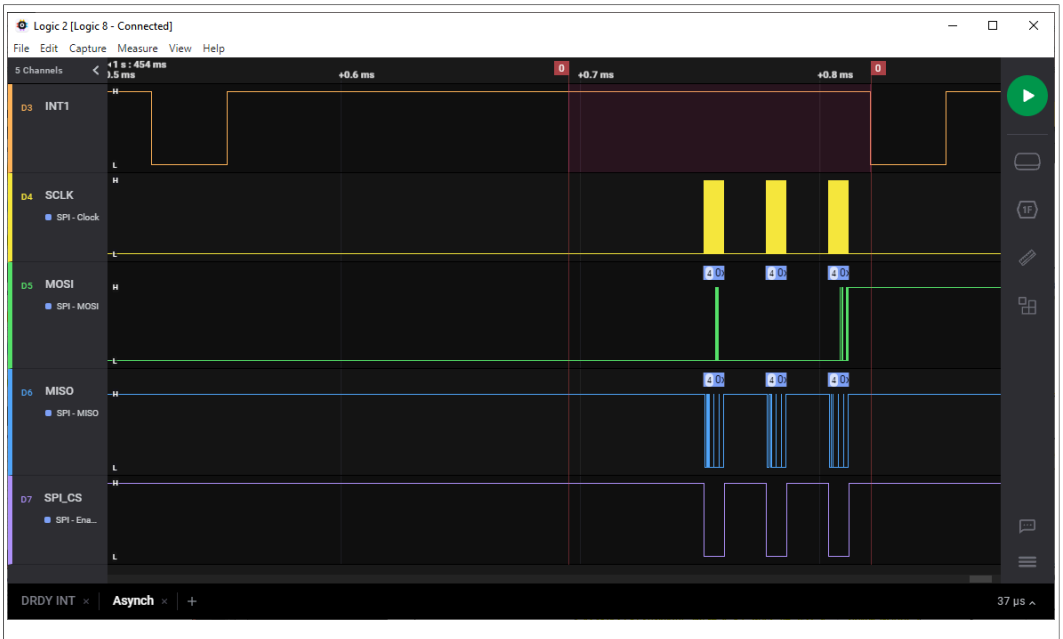

Figure 2. INT1 and SPI signals: Asynchronous data reading

Several specific conditions need to exist for the error to present, which means the statistical occurrence is very low, especially when the traffic on the serial interface is minimal.

In order to eradicate this communication noise, a reliable workaround is described in this document. Alternatively, if the workaround cannot be deployed, a few suggestions are provided to mitigate its impact.

3.1.3 Workaround

The susceptibility of the measurement to induced noise is reduced by minimizing the communication traffic on the serial interface during the measurement phase of the sensor.

Configure the system such that the host MCU collects sensor data using data ready interrupts before the next measurement phase begins. See Figure 3 and Figure 4.

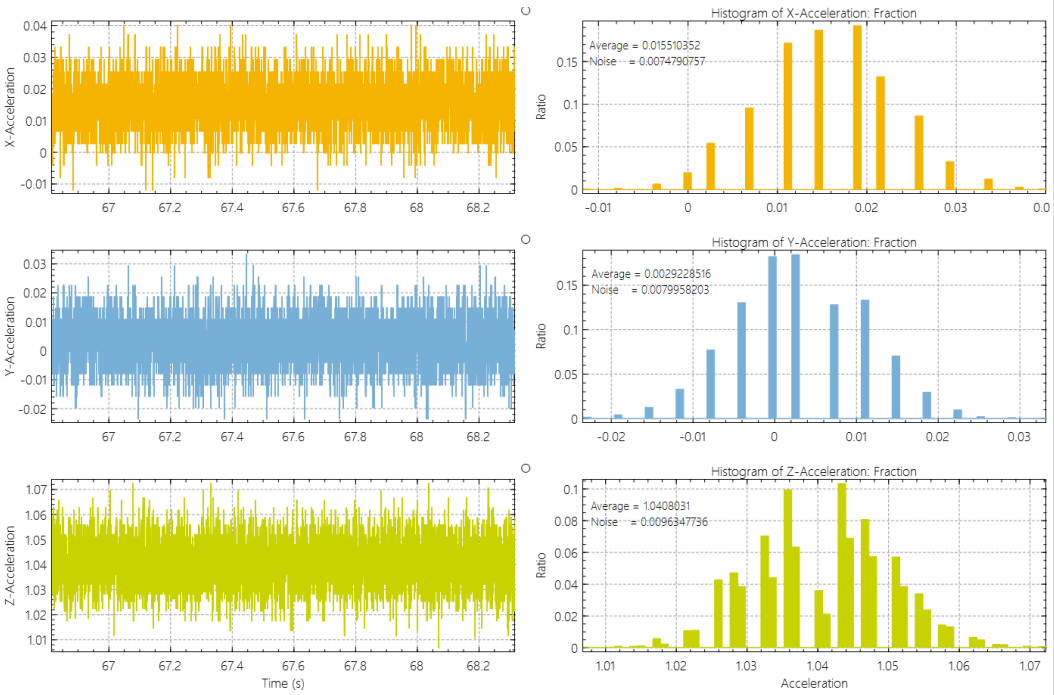

Figure 3. Acceleration Data (in g): Plot vs Time and Histogram, synchronous data reading based on DRDY interrupt

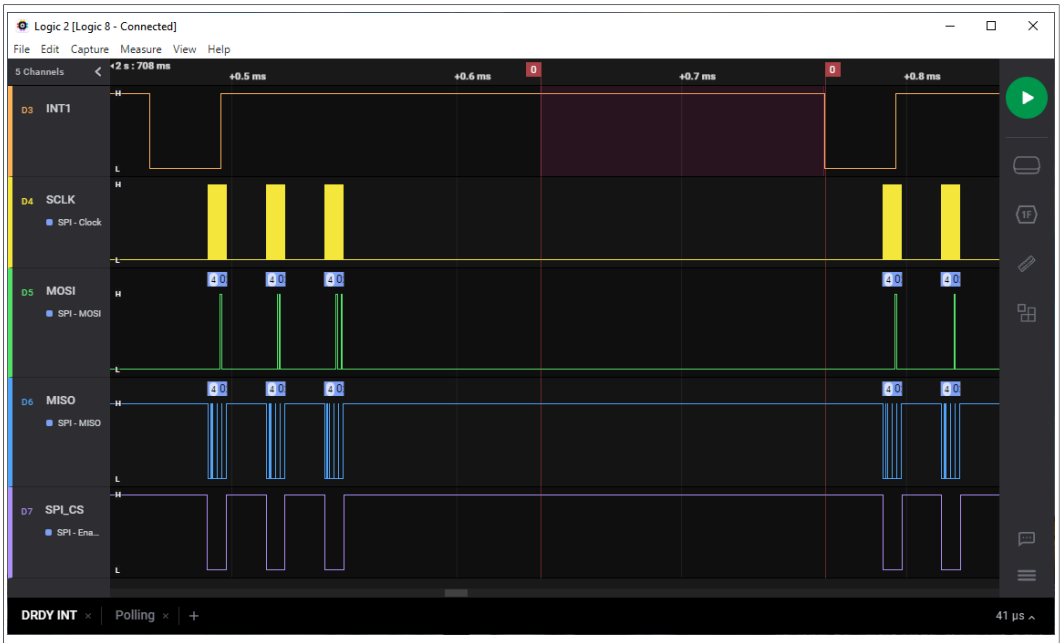

Figure 4. INT1 and SPI signals: synchronous data reading based on DRDY Interrupt

3.1.3.1 Sensitive window

The AFE measurement sequence takes about 126 µs total, but only 3 very small time slices within this phase (<0.5 µs cumulated duration) are sensitive to the digital signal transitions. This explains the sporadic behavior of communication glitches, rarely encountered on consecutive samples.

This AFE measurement time window is shown between the 2 pink vertical time bars (marked with a 0 flag) on Figure 2 and Figure 4.

3.1.3.2 Using data ready interrupts

The data ready interrupt in FXLS8967AF and FXLS8974CF is enabled using the INT_EN register (address 20h) and INT_PIN_SEL register (address 21h) (see Table 3 and Table 4).

1. Enable **INT_EN[**DRDY_EN**]**.
2. Map the data ready interrupt to one of the INTx pins available on the device. Set DRDY_INT2 bit to route data ready interrupt to INT2 pin or clear the bit to route to INT1 pin.

Note: *In the case of BT_MODE = V_{DD} (motion detect mode), only INT1 pin can be used. The INT2 pin function is reserved for the boot output pulse and, therefore, is not available for this purpose.*

*Also, when the INT2 pin is configured for the external trigger function, for example, when **SENS_CONFIG4[**INT2_FUNC**]** = 1, a logic 1 value in DRDY_INT2 bit field is ignored.*

Table 3. INT_EN register (address 20h)

Bit	7	6	5	4	3	2	1	0
Name	DRDY_EN	BUF_EN	SDCD_OT_EN	SDCD_WT_EN	ORIENT_EN	ASLP_EN	BOOT_DIS	WAKE_OUT_EN
Reset[1]	0	0	0	0	0	0	0	0
Reset[2]	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] BT_MODE = 0
[2] BT_MODE = 1

Table 4. INT_PIN_SEL register (address 21h)

Bit	7	6	5	4	3	2	1	0
Read	DRDY_INT2	—	SDCD_OT_INT2	SDCD_WT_INT2	ORIENT_INT2	ASLP_INT2	BOOT_INT2	WAKE_OUT_INT2
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

3.1.3.3 Time window to perform serial communication after receiving data ready interrupt

Upon reception of the data ready interrupt on the selected interrupt pin, the host must quickly perform a burst read of the data registers before the next measurement cycle begins for the successive data sample. This ensures the bus communication associated with reading the current data sample does not couple noise to the successive data sample measurement.

In addition, if FXLS8967AF and FXLS8974CF are used in a shared I^2C/SPI bus along with other devices, the communication with other devices must complete before the next measurement cycle in FXLS8967AF and FXLS8974CF begins, in order to prevent bus traffic from inducing noise to the sensor measurement.

In order to minimize the duration of the data registers reading, it is recommended to use the SPI communication interface with a fast Clock frequency. Maximum value supported by the sensor is 4 MHz.

Table 5. Measurement phase timings

Sample size = 30

Mean (µs)	Standard deviation (µs)
126.1	0.88

Table 6 identifies the maximum time window (from the starting edge of the data ready interrupt) within which all the serial communications must complete before the measurement phase for the next sample begins.

Table 6. Time window allowed for serial communications after the rising edge of the data ready interrupt

Average value from 30 samples.

Mode	Time (µs)
LPM (ODR dependent)	$Time\ \ window = \frac{1.0 \times 10^6}{1.1 \times ODR} - 1.1 \times measurement\ \ phase$ where: measurement phase = 126.1 µs (Table 5),
HPM	$Time\ \ window = \frac{1.0 \times 10^6}{1.1 \times 3200} - 1.1 \times measurement\ \ phase = 145.38$ where: measurement phase = 126.1 µs (Table 5),

For example, with the device operating with ODR = 200 Hz in LPM mode, the time window allowed for serial communications after the starting edge of the DRDY interrupt = 4406 µs.

3.1.4 Mitigation

3.1.4.1 Use a low voltage supply

Communication-induced glitches are basically absent when operating at V_{DD} = 1.8 V so a low supply is preferred to avoid risk of data spikes.

3.1.4.2 Use SDCD debounce counter

When using SDCD event detection, and in particular SDCD Outside Threshold detection, the communication glitch may cause a false positive event to be raised. In that case, setting a small debouncing count in SDCD_OT_DBCNT register helps to reject such potential sporadic spikes due to communication noise.

3.1.4.3 Use HPM decimation

When sensor measurement mode is set to HPM, internal averaging and decimation are performed. This means that impact of a potential glitch is diluted by the averaging process. High decimation (low ODR) is recommended, whenever possible.

3.1.4.4 Use removal algorithm

Communication glitches can be considered as outliers, therefore standard algorithms to remove outliers are suitable to discard them.

3.1.5 Fix plan

None.

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Tables

Tab. 1. Device identification table 3
Tab. 2. Functional problems table 3
Tab. 3. INT_EN register (address 20h) 7
Tab. 4. INT_PIN_SEL register (address 21h) 7
Tab. 5. Measurement phase timings 7
Tab. 6. Time window allowed for serial communications after the rising edge of the data ready interrupt 7

Figures

Fig. 1. Acceleration data (in g): Plot vs Time and Histogram, asynchronous data reading 4
Fig. 2. INT1 and SPI signals: Asynchronous data reading 4
Fig. 3. Acceleration Data (in g): Plot vs Time and Histogram, synchronous data reading based on DRDY interrupt 5
Fig. 4. INT1 and SPI signals: synchronous data reading based on DRDY Interrupt 6

Contents

1 Product identification 3
2 Errata overview 3
3 Functional problems detail 3
3.1 E1: Communication noise 3
3.1.1 Introduction 3
3.1.2 Problem 3
3.1.2.1 Measurement details for figures 3
3.1.3 Workaround 5
3.1.3.1 Sensitive window 6
3.1.3.2 Using data ready interrupts 6
3.1.3.3 Time window to perform serial communication after receiving data ready interrupt 7
3.1.4 Mitigation 8
3.1.4.1 Use a low voltage supply 8
3.1.4.2 Use SDCD debounce counter 8
3.1.4.3 Use HPM decimation 8
3.1.4.4 Use removal algorithm 8
3.1.5 Fix plan 8
4 Legal information 9

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