IMXRT500HDG

i.MX RT500 Hardware Design Guide

Rev. 0 — 15 November 2022 **User guide**

Document information

Information	Content
Keywords	IMXRT500HDG, i.MX RT500, MIMXRT595-EVK
Abstract	This user guide provides details about the system hardware design to help the users to develop their i.MX RT500 based designs

1 Introduction

This user guide provides details about the system hardware design to help the users to develop their i.MX RT500 based designs. Recommendations and examples from the NXP MIMXRT595-EVK board are also included in the following section to illustrate the concepts.

1.1 MIMXRT595 hardware design guidelines overview

This section provides an overview of MIMXRT595 hardware design guidelines and lists the detailed description of:

- Power domains: Multiple power domains on the chip and how to filter or decouple them
- External clocks: External system clocks that are available on the chip
- Debug, trace, scan, and programming: Connections review
- Layout recommendations: Requirements for EVK layout

For more details, see Figure 1.

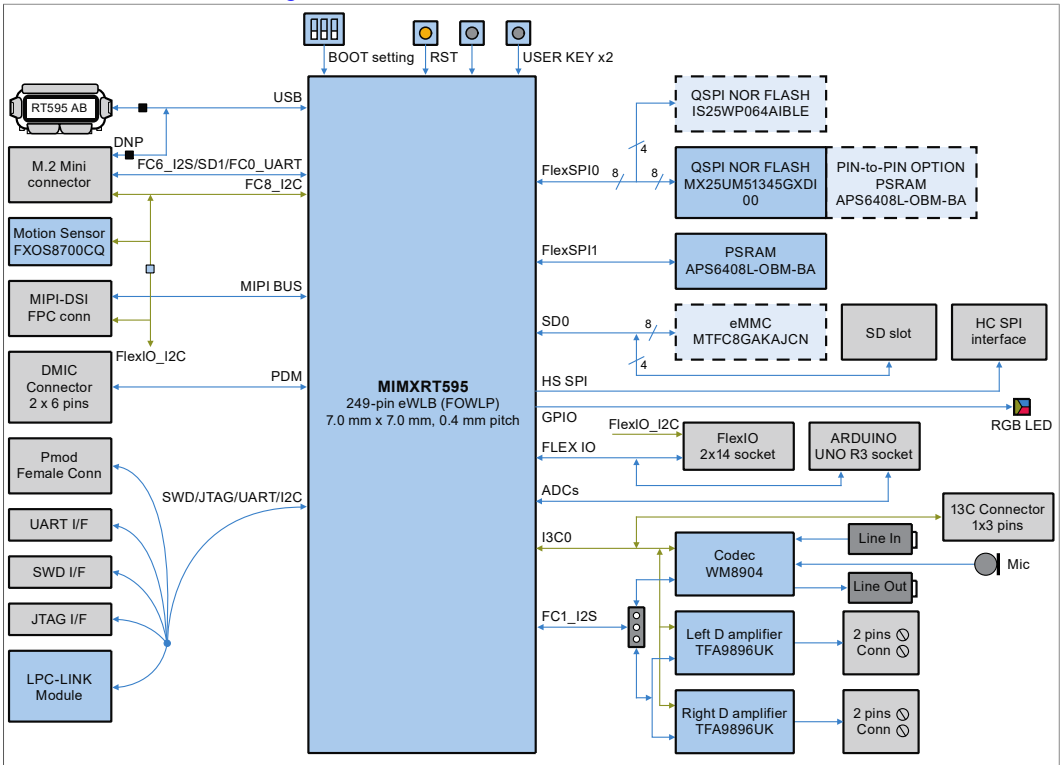


Figure 1. MIMXRT595 block diagram

Key features:

- 28FDSOI Technology
- Cortex M33
- Fusion F1 DSP
- Graphics Subsystem
- 5 MB Low Leakage SRAM
- Connectivity
- Timers

Operating characteristics:

- Power supply:
  - VDDCORE: 0.6 V to 1.155 V
  - VDDIO_0/1/2/4: 1.71 V to 1.89 V
  - VDDIO_3: 1.71 V to 3.6 V
- Temperature range (ambient): -20 C° to +70 C°

2 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Acronym	Definition
BGA	Ball Grid Array
CLKIN	Clock-In
CMOS	Complementary Metal-Oxide-Semiconductor
FOWLP	Fan-Out Wafer-Level Package
GPIO	General-Purpose Input/Output
HDI	High Density Interconnect
ISP	In-System Programming
ITM	Instrumentation Trace Macrocell
LDO	Low-Dropout Regulator
MCU	Microcontroller Unit
MLCCs	Multi-layer Ceramic Capacitors
OTP	One-Time-Programmable
PCB	Printed-Circuit board
PFM	Pulse-Frequency Mode
PMIC	Power Management IC
PWM	Pulse Width Modulation
PIU	Port Interface Unit
QFN	Quad Flat-pack No Lead
QSPI	Quad Serial Peripheral Interface
RTC	Real-Time Clocks
SDIO	Secure Digital I/O
SWD	Serial Wire Debug
SWO	Serial Wire Output
SWC	Serial Wire Clock
WLCSP	Wafer-Level Chip-Scale Package
WLCSP	Wafer-Level Chip-Scale Package
XTAL	Crystal

3 Power domains

This section provides details about the power domains on the chip and in the system.

3.1 i.MX RT500 power domains always-on, GPIO, and analog

The i.MX RT500 has several digital and analog supplies to power internal circuits and the GPIO ports that interface to the system. Table 2 lists the power rails; minimum, maximum, and typical voltages for each power rail.

Note: *The minimum recommended filtering for each supply, including the bulk storage and local decoupling capacitors; and a short description of the domain supply.*

- VDD_AO1V8 is a low power always-on supply that powers the internal modules and system registers that keep the chip ready to respond to low-power wake-up events. These include the real-time clock module, general-purpose registers, the RESETN input, and PMIC control pins.
- The chip has five separate GPIO power domains that are used to source I/O functions around the chip. All five I/O power rails operate at 1.8 V, and one (VDDIO_3) can operate at 3.3 V as well.
- The VDD1V8 power rail supplies on-chip analog functions.

Table 2. Power rails

Power rail	MIN (V)	TYP (V)	MAX (V)	Decoupling and bulk capacitors (min qty)	Description
VDD_AO1V8	1.71	1.8	1.89	1 × 0.22 µF + 1 × 1 µF	1.8 V supply for always-on features. It includes the RTC module, general-purpose GPREG[7:0] registers, and the RESETN and PMIC control pins (LDO_ENABLE, PMIC_IRQ_N, PMIC_MODE0, and PMIC_MODE1).
VDDIO_0	1.71	1.8	1.89	3 × 0.22 µF + 1 × 10 µF	1.8 V power supply for GPIOs
VDDIO_1	1.71	1.8	1.89	3 × 0.22 µF + 1 × 10 µF	1.8 V power supply for GPIOs
VDDIO_2	1.71	1.8	1.89	1 × 0.22 µF + 1 × 1 µF	1.8 V power supply for GPIOs
VDDIO_3	1.71	1.8	1.89	1 × 0.22 µF + 1 × 1 µF	1.8 V or 3.3 V power supply for GPIOs
	3.0	3.3	3.6		
VDDIO_4	1.71	1.8	1.89	1 × 0.22 µF + 1 × 1 µF	1.8 V power supply for GPIOs
VDD1V8 VDD1V8_1	1.71	1.8	1.89	5 × 0.22 µF + 1 × 10 µF	1.8 V supply voltage for on-chip analog functions. VDD1V8_1 powers the On-Chip OTP Control module.

3.2 i.MX RT500 power domains, ADC, and CORE logic supplies

1. The ADC operates at 1.8 V and can only measure up to the VDDA level, see in the VDDA_ADC1V8 row of Table 3.
2. The VDDCORE is the internal core logic supply that requires a 1.0 V for Power-On and can be changed in the application.

The minimum voltage is 0.7 V in active mode to save power, but the level can be reduced in retention mode. This supply requires quite a bit of decoupling capacitance. Refer the following steps on how to apply the minimum quantity of capacitors across the 12 of VDDCORE pins.

- When LDO_ENABLE is externally tied low, the user must boot at VDDCORE = 1.0 V or higher (low-power/normal clock mode - OTP setting - BOOT_CLK_SPEED) or VDDCORE = 1.13 V (High-Speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the VDDCORE can be adjusted to the desired level.
- When LDO_ENABLE is externally tied high, the on-chip regulator to the VDDCORE core voltage in PMC is set to the default value of 1.05 V (low-power/normal clock mode - OTP setting - BOOT_CLK_SPEED) or 1.13 V (high-speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the POWER_SetLdoVoltageForFreq API function can be used internally to configure the on-chip regulator voltage for the VDDCORE.
- When performing any OTP read/write function, the VDDCORE voltage must be set to 1.0 V or higher when LDO_ENABLE is externally tied high or low.

3. For the ADC analog reference, VREFP is a 1.8 V reference that must be the same level as for VDDA_ADC1V8.

Table 3. ADC and CORE logic supplies

Power rail	MIN (V)	TYP (V)	MAX (V)	Decoupling and bulk capacitors (min qty)	Description
VDDA_ADC1V8	1.71	1.8	1.89	1 × 0.22 µF	1.8 V analog supply voltage for ADC.
VDDA_BIAS	1.71	1.8	1.89	1 × 0.22 µF + 1 × 1 µF	For ADC and comparator input range from 0 – 1.8 V
VDDCORE	0.6	1.0	1.155	5 × 0.22 µF + 1 × 10 µF	The minimum voltage is 0.6 V in retention mode, and 0.7 V in active mode.
	0.7	1.0	1.155		Power supply for core logic may be supplied from the on-chip regulator or by an off-chip PMIC. External filter capacitors are always required on these pins. For details, see the power connection information for values and other recommendations.
	1.0	1.0	1.155		The minimum voltage of 1.0 V is required for initial power on
VREFP	1.71	1.8	1.89	1 × 0.22 µF	ADC positive reference voltage input

3.3 i.MX RT500 power domains, internal regulator

The LDO_ENABLE input signal is listed in this power domain section because it is the control signal that enables the internal VDDCORE LDO regulator when an external VDDCORE supply is not used. This pin is pulled high to enable the internal LDO and tied low when an external supply provides VDDCORE. Refer to Section 3.6.

Along with the minimum quantities of bulk and decoupling capacitors, we must see Note on where to place the capacitors and parametric recommendations for the capacitors.

In the high-speed designs, which use ball-grid array packaging, the balls are soldered to the top layer, the signals are routed on at least two layers, and the power pins are routed on two or more other layers. The area directly below the MCU on the bottom layer is where most, if not all, of the decoupling capacitors should be connected to the ground and power domains.

Capacitor package size, tolerance, rated voltage, and dielectric recommendations are presented for the three main capacitors used in the decoupling networks, see Table 4. Capacitor information is presented in the Section 7.

Table 4. Capacitor information

Signal	Description
LDO_ENABLE	This input enables the on-chip regulator to power core logic through the VDDCORE pins when high. Tie low if an off-chip PMIC is used to supply power to the core logic. This pin cannot be left floating. A 100 kohm external pull-up or 10 kohm external pull-down resistor is recommended.

Note:

1. *Decoupling and bulk capacitors must be placed on the bottom side of the PCB, underneath the MCU for the smallest loops.*
   - *For the 0.22 µF capacitors, use the 0201 packages, 10 V, 20 %, X5R, or X7R*
   - *For the 1 µF capacitors, use the 0402 packages, 10 V, 10 %, X5R, or X7R*
   - *For the 10 µF capacitors, use the 0603 packages, 16 V, 20 %, X5R, or X7R*
     Note: *The 0805 package is acceptable.*

3.4 Power domains for GPIO

Table 5 lists the GPIO in the specific VDDIO and VDD_AO1V8 domains.

Table 5. Domains

VDDIO rail	GPIO pins
VDDIO_0	PIO0_0 to PIO0_13
	PIO1_11 to PIO1_15
	PIO1_18 to PIO1_29
	PIO2_14 to PIO2_15
	PIO3_25 to PIO3_29
	PIO4_0 to PIO4_6
	PIO6_27

Table 5. Domains*...continued*

VDDIO rail	GPIO pins
VDDIO_1	PIO0_14 to PIO0_19
	PIO0_21 to PIO0_25
	PIO0_28 to PIO0_31
	PIO1_0
	PIO1_3 to PIO1_7
	PIO1_9 to PIO1_10
	PIO2_24 to PIO2_31
	PIO3_1 to PIO3_3
	PIO4_11 to PIO4_17
	PIO4_18
	PIO5_4, PIO5_8
	PIO5_15 to PIO5_18
	PMIC_I2C_SCL
	PMIC_I2C_SDA
VDDIO_2	PIO1_30 to PIO1_31
	PIO2_0 to PIO2_8
	PIO2_9 to PIO2_11
VDDIO_3	PIO4_20 to PIO4_31
	PIO5_0 to PIO5_3
VDDIO_4	PIO3_8 to PIO3_18
	PIO3_19 to PIO3_21
VDD_AO1V8	RESETN
	LDO_ENABLE
	PMIC_IRQ_N
	PMIC_MODE0 and PMIC_MODE1
	RTCXIN and RTCXOUT

- `VDDIO_0`, `VDDIO_1`, `VDDIO_2`, and `VDDIO_4` supplies can be powered between 1.71 V to 1.89 V.
- `VDDIO_3` can be powered between 1.71 V and 3.6 V.

3.5 Power-on sequence using PMIC (internal LDO disabled)

The internal and external power rails must follow a sequence to avoid start-up issues. These sequences using a PMIC for the `VDDCORE` node, with the internal `CORE LDO` disabled, and external supplies with the internal `VDDCORE` regulator enabled are similar.

1. The always-on supply must be powered first or in conjunction with the `VDD1V8` supplies which power the main digital functions that initialize the MCU.

2. PMIC mode pins are the outputs that are controlled by an always-on supply. These pins must have external pullups to VDD_AO1V8 and get validated after several microseconds once VDD_AO1V8 is stable.
3. The VDDA_ADC1V8 supply and VREFP reference are powered-up at the same time as VDD1V8 or later.
4. The VDDIO rails and VDDA_BIAS are also powered at the same time as VDD1V8 or later.
   CAUTION: *When VDDIO_3 is 3.0 V, there must be a delta of not more than 1.89 V during the rampup.*
5. VDDCORE is powered last by the PMIC, which handles the power sequencing.
   Note: *When LDO_ENABLE is externally tied low, the user must boot at VDDCORE = 1.0 V or higher (Low-power / Normal clock mode - OTP setting - BOOT_CLK_SPEED) or VDDCORE = 1.13 V (High-Speed clock - OTP setting - BOOT_CLK_SPEED).*
   Thereafter, the VDDCORE can be adjusted to the desired level. The PMIC also provides the RESETN deassertion after VDDCORE is stable.

When a PMIC is not used, enable the internal VDDCORE LDO to provide VDDCORE. The PMC releases RESETN internally when VDDCORE is stable.

Note: *For ERR050716, generally, all 1.8 V power pins are supplied by the same regulator, so all are applied at the same relative time. Decoupling capacitor charging delays are not considered to be significant when all the 1.8 V domains are powered at the same time.*

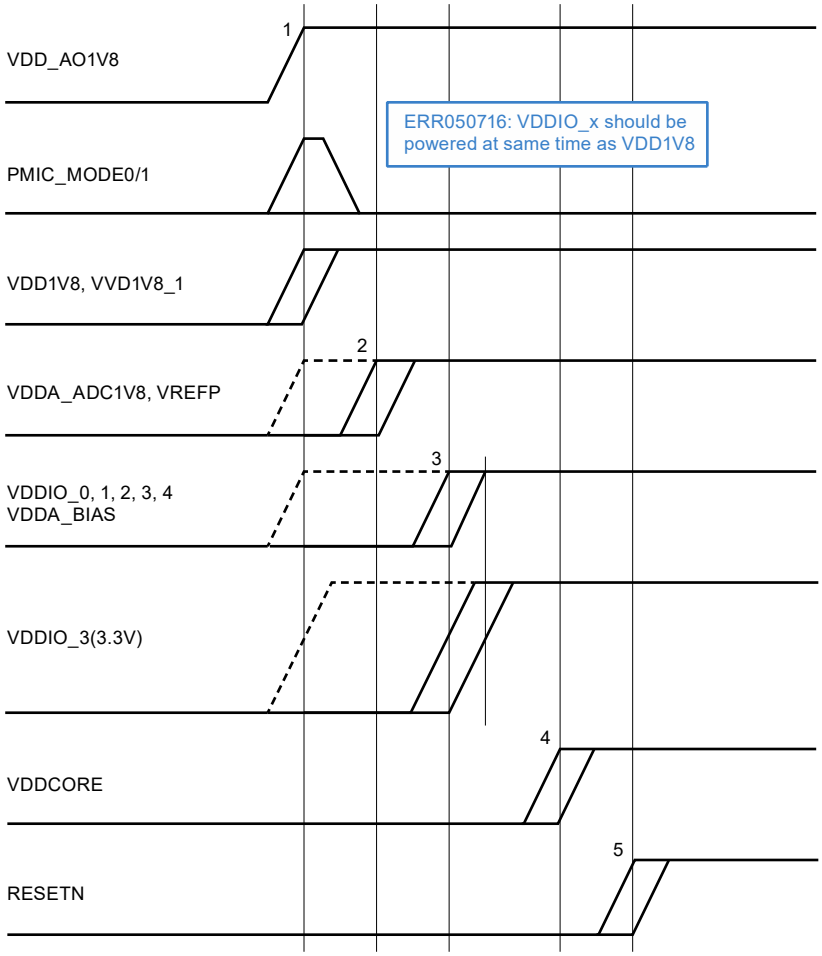


Figure 2. Power-on sequence

The power-on sequences are shown in the Figure 2 are as follows:

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 should be powered first. If using PMIC, mode pins are pulled-up to always-on supply until mode pins are active.
2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later.
3. VDDIO_x and VDDA_BIAS can be powered concurrently with VDD1V8 range or later. The delta voltage between VDDIO_3 and VDD1V8 must be 1.89 V or less when VDDIO_3 is 3.3 V.
4. Power-up VDDCORE should not be ramped-up until after all the other supplies have completed the rampup.
5. Hold RESETN low until VDDCORE is valid when PMIC is used. The only difference when using internal VDDCORE LDO (LDO_ENABLE = 1) is that internal PMC releases internal RESETN when VDDCORE is stable.

3.6 NXP PCA9420 PMIC

The NXP PCA9420 PMIC designed to be used with the i.MX RT500 and i.MX RT600 microcontrollers. This PMIC has two LDO regulators and two switch-mode regulators.

This PMIC is available in two small packages:

- BGA-style wafer level chip scale package WLCSP
- 24-pin quad flat pack, no leads QFN

The block diagram shown in Figure 3 has taken from the PCA9420 data sheet.

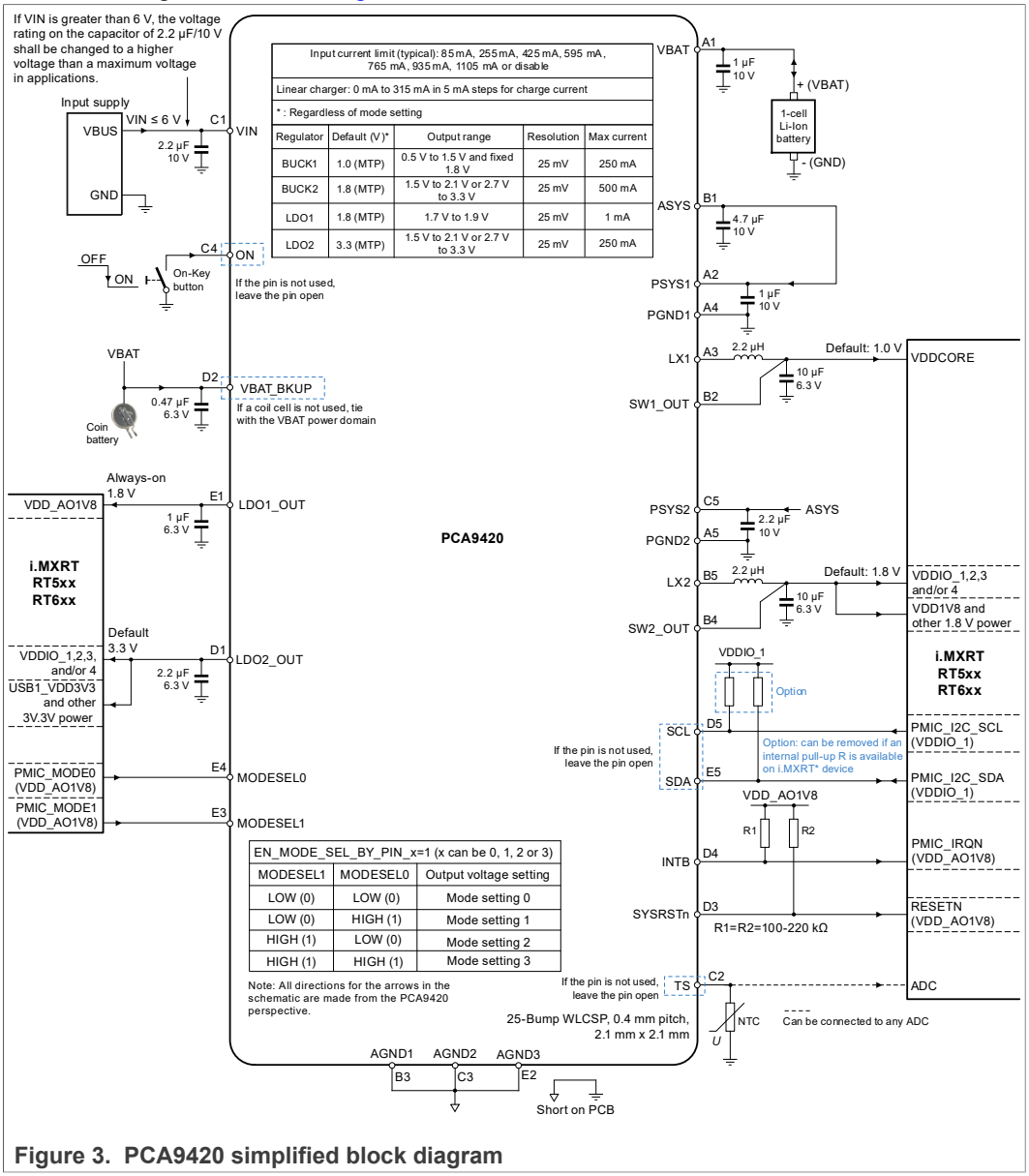


Figure 3. PCA9420 simplified block diagram

- Power Management IC for low-power microcontroller applications
- Two LDO regulators and two switch-mode regulators
- 5 x 5 bump WLCSP or 24-pin QFN package −EVK uses the WLCSP package

3.7 MIMXRT595-EVK PMIC supply assignments

Figure 4 focuses on the output portion of the PCA9420 PMIC, as we see the two LDO outputs on the left and the two switching outputs on the right.

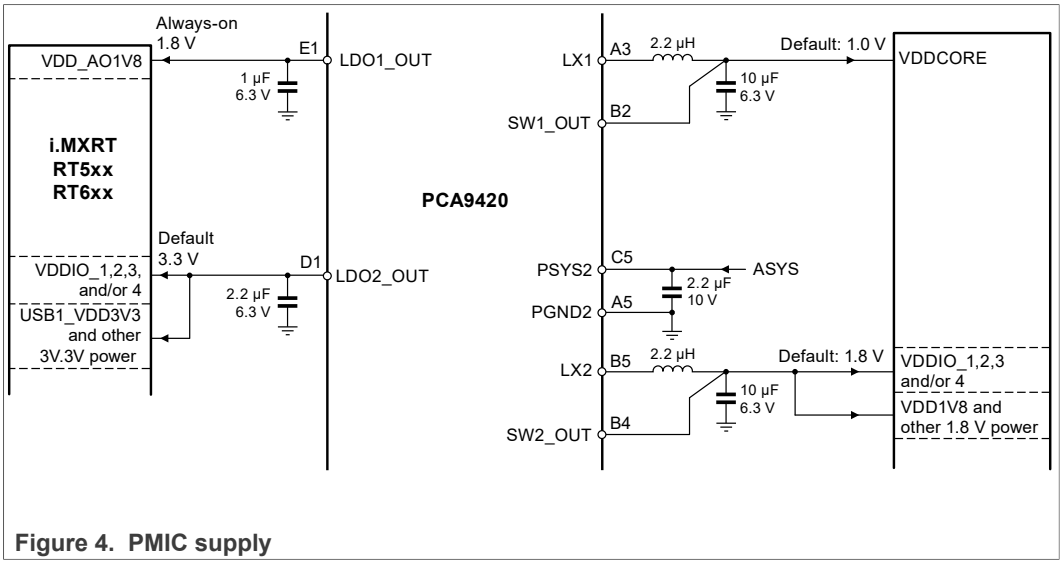


Figure 4. PMIC supply

Table 6. PMIC supply

PMIC Supply	Description	Power rail
LDO1_OUT	Low power always-on 1.8 V supply	VDD_AO1V8
LDO2_OUT	3.3 V supply	USB1_VDD3V3, VDDA_BIAS, VDDIO_3
SW1_OUT	1.0 V core supply	VDDCORE, MIPI_DSI_VDD11
SW2_OUT	High current 1.8 V supply	VDD1V8, VDD1V8_1, VDDIO_0, VDDIO_1, VDDIO_2, VDDIO_3, VDDIO_4, VDDA_ADC1V8, VREFP

- `LDO1_OUT` is configured as the low power always-on supply, which also biases the RESETN and PMIC control signal pull-up resistors.
- `LDO2_OUT` is configured as the main 3.3 V supply for the USB module, and the `VDDIO_3` domains.
- `SW1_OUT` is configured to provide the 1.0 V CORE supply, which is also used by the `MIPI_DSI` module.
- `SW2_OUT` is the high current 1.8 V supply that powers the remaining 1.8 V domains and loads.

Note: *The `SW2 _OUT` operates in Pulse-Frequency Mode (PFM) under low load conditions (less than 50 mA) for power efficiency and 1 MHz Pulse Width Modulation (PWM) mode for higher loads. In the low load condition, PFM operation generates more than 20 mV of ripple on this supply, which can propagate to the main oscillator and cause a jitter. If the MCU operates under low load conditions and clock jitter is not acceptable, an external 1.8 V LDO regulator must be used for the `VDD1V8` supply.*

Note: *You can request specific default power supply voltages and sequences for the PMIC and the PMIC team generates a new part number for you.*

4 i.MX RT500 power domains, other power rails

Other power rails include:

- USB 3.3 V supply
- 1.1 V MIPI_DSI_VDD11 supply for the MIPI_DSI digital core (which we recommend tying to the VDDCORE supply)
- 1.8 V MIPI_DSI_VDD18 supply for the MIPI_DSI PHY
- 1.8 V MIPI_DSI_VDD18_VDDA_CAP domain, which requires a stabilization capacitor for this internal domain
- USB1_VBUS is a 3 V to 5 V signal from the USB connector, which is used to detect the presence of an active USB cable. This is an input rather than a power rail.
- There are several internal VSS connections VSS, VSSA, MIPI_DSI_VSS, and VREFN that must be tied to a common ground node.

Regarding the termination of unused pins, see Table 7. For more details, see Section "Termination of unused pins" of *i.MX RT500 Low-Power Crossover Processor Data Sheet with Addendum* (document IMXRT500EC).

Table 7. Other power rails

Power rail	MIN (V)	TYP (V)	MAX (V)	Decoupling and bulk capacitors (min qty)	Description
USB1_VDD3V3	3.0	3.3	3.6	1 × 0.22 µF	USB1 analog 3.3 V supply
USB1_VBUS	3.0	5.0	5.5	1 × 0.22 µF	USB1_VBUS input to validate USB presence
MIPI_DSI_VDD11	0.85	1.1	1.155	1 × 0.22 µF	MIPI DSI 1.1 V digital core input voltage supply. Recommend trying to VDDCORE voltage.
MIPI_DSI_VDD18	1.71	1.8	1.89	1 × 0.22 µF	MIPI DSI 1.8 V PHY I/O input voltage supply
MIPI_DSI_VDD18_VDDA_CAP	—	—	1.155	1 × 0.22 µF	Internal domain
VREFN	—	0	—	—	ADC negative reference voltage. Tie to GND
VSSA	—	0	—	—	Analog negative supply. Tie to GND
VSS	—	0	—	—	MCU negative supply. Tie to GND
MIPI_DSI_VSS	—	0	—	—	MIPI_DSI_VSS. Tie to GND

5 External clocks

This section provides details about the crystal oscillators, external clock input, and versatile CLKOUT output.

5.1 External clocks

The main crystal oscillator (XTALIN / XTALOUT) can drive crystals from 4 MHz to 32 MHz.

The main crystal oscillator can operate in low-power or high gain modes, while the possible frequency range is 4 MHz to 32 MHz, the practical range is 5 MHz to 26 MHz due to limitations of the on-chip PLLs.

The Real-Time Clock (RTC) oscillator (RTCXIN / RTCXOUT) is strictly for:

- 32 kHz real-time clock (RTC) that can be used as a system clock and as timer clocks
- Internal load capacitor selection 32.768 kHz crystals

It operates in low-power mode only and has internal load capacitor banks to tune the crystal frequency, which can reduce component count.

CLKIN and CLKOUT functions:

- CLKIN input clock – alternate input clock
- CLKOUT output clock:
  - Convenient output clock to measure crystal or system frequencies
  - Use to tune system and RTC oscillators

5.2 Main crystal oscillator (XTALIN/XTALOUT)

The main crystal oscillator uses the dedicated XTALIN and XTALOUT pins. This high-frequency oscillator is used to source the PLLs and internal system clocks.

For the PLL multipliers, which limit the practical range of crystal frequencies, see Table 8. There is a limitation for the PLL crystal oscillator as it has a range from 5 MHz to 26 MHz crystal, with a PLL multiplier range of 16 through 22, yielding a VCO frequency range of 80 MHz to 572 MHz. This oscillator has a low-power mode that starts up with a normal gain and automatically adjusts to a lower gain to sustain oscillation. This mode provides the lowest oscillator power dissipation but can be susceptible to noise if the system is electrically noisy. The low-power oscillator configuration has its internal feedback resistor, so an external feedback resistor is not necessary or recommended.

The high gain oscillator is a normal gain amplifier that does not adjust its drive level. The high gain mode requires an external 1 M ohm feedback resistor. The high gain mode is less susceptible to system noise but consumes more power.

Each configuration, low-power and high gain, requires external load capacitors on the crystal pins, see Figure 5. For more details on oscillator load capacitance, refer to Section 5.9.

This oscillator can be channeled to the CLKOUT output to measure the frequency and trim the load capacitors as necessary. This oscillator can also be bypassed by driving an external clock signal into the XTALIN pin.

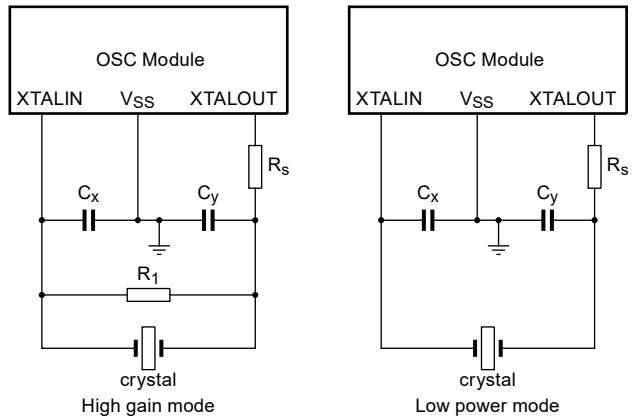


Figure 5. High gain and low-power modes

Table 8. PLL frequency

PLL frequency (MHz) based on multiplier							
Crystal (MHz)	**16**	**17**	**18**	**19**	**20**	**21**	**22**
4	64	68	72	76	80	84	88
5	80	85	90	95	100	105	110
8	128	136	144	152	160	168	176
10	160	170	180	190	200	210	220
16	256	272	288	304	320	336	352
20	320	340	360	380	400	420	440
24	384	408	432	456	480	504	528
26	416	442	468	494	520	546	572
32	512	544	576	608	640	672	704
VCO range is from 80 MHz to 572 MHz.							

5.3 Main crystal oscillator (XTALIN/XTALOUT), at high gain mode

The high gain mode is the default setting at reset. The oscillator requires software configuration, so it does not start up at power-up until firmware initializes the oscillator. The high gain mode requires the 1 M ohm feedback resistor and external load capacitors, see Figure 6.

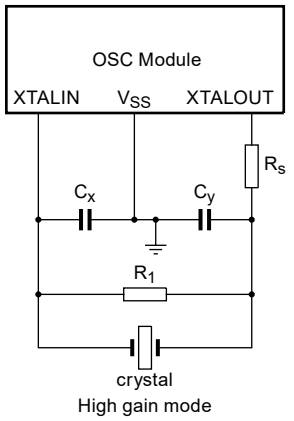


Figure 6. High gain mode

Note: *The series resistor is in the XTALOUT leg. A small value resistance may be used for low frequency (<8 MHz) crystals, but it is normally not needed.*

While the high gain mode is capable of driving lower frequency crystals with rail-to-rail levels, the levels are attenuated somewhat at higher frequencies. Use high gain mode when operating in noisy environments. This is more tolerant of noise and reduces system clock jitter.

However, the high gain mode could also have higher emissions if the oscillator is not loaded properly. Too little load capacitance can cause higher frequency operation.

5.4 Main crystal oscillator (XTALIN/XTALOUT) at low-power mode

Low-power mode is selected with an enable bit in the oscillator control register. The low-power configuration has an internal feedback resistor, an external feedback resistor is not required or recommended. The low-power mode oscillator requires external load capacitors to tune the crystal oscillator frequency. Low-Power mode is selected by setting the `LP_ENABLE` bit in `SYSOSCCTL0`. Low-Power mode saves energy by reducing the drive current after initial oscillation:

- Oscillation levels are around 0.8 V peak-to-peak
- Do not attempt to measure the oscillation levels

As mentioned earlier, the low-power mode starts with a normal gain drive and then reduces the gain automatically to sustain oscillation. The gain control circuit can also increase gain, if necessary, to sustain oscillation. While the crystal signals can be measured in low-power mode, attaching a scope probe to either of these pins which alter the gain characteristics, amplitude, wave shape, and frequency. In general, it is best to avoid probing the oscillator pins (in any mode) and use the CLKOUT function to tune the oscillator frequency. The low-power oscillator consumes microampere instead of milliampere as in high gain mode, so power savings are significant in low-power modes, see Figure 7.

Note: *The series resistor is in the XTALOUT leg, is not recommended for the low-power oscillator. It is a part of the pierce oscillator circuit convention.*

Due to the smaller oscillation waveforms, the low-power configuration becomes more sensitive to system noise and can produce more jitter due to the reduced amplitude.

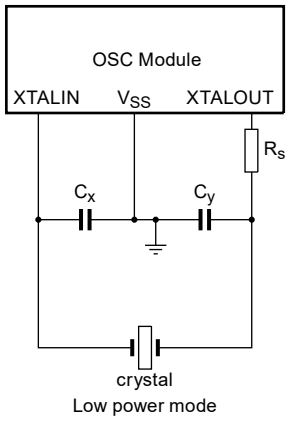


Figure 7. Low-power mode

5.5 Main crystal oscillator (XTALIN/XTALOUT) bypass mode

The main crystal oscillator can be bypassed with an external oscillator.

It is recommended to:

1. Connect a 1.8 V CMOS-level crystal oscillator (called XO) to the XTALIN input and float the XTALOUT output.
2. Enable the high gain oscillator by clearing the `LP_ENABLE` bit in the system oscillator control register `SYSOSCCTL0`.
3. Set the `BYPASS_ENABLE` bit in `SYSOSCCTL0` to enable the bypass.

The CLKIN input, available on several GPIO pins, can also bypass the main oscillator, if desired, without using this bypass mode.

This oscillator's bypass mode is not compatible with temperature-compensated crystal oscillators `TCXO` that have clipped sine-wave outputs. However, a clipped sine-wave `TCXO` can be used without the bypass mode when the low-power oscillator is enabled.

1. Connect the `TCXO` output (800mVp-p minimum) to the `XTALIN` input and float `XTALOUT`.
2. Enable the low-power oscillator by setting the `LP_ENABLE` bit in the system oscillator control register, `SYSOSCCTL0`.
   Note: *Do not set the `BYPASS_ENABLE` bit.*

The AC coupling capacitor (also called DC-cut capacitor) is `TCXOs`, generally it is not needed when the low-power oscillator is used since the oscillator has its internal coupling capacitor.

5.6 Real-time Clock (RTC) oscillator (RTCXIN/RTCXOUT)

The RTC is a low-power oscillator developed for 32.768 kHz crystals. Its output can be gated to the system clock. For more details, see Figure 8.

- The RTC oscillator uses the dedicated `RTCXIN` and `RTCXOUT` pins.
- The RTC oscillator has an internal feedback resistor. An external feedback resistor is not required or recommended. RTC oscillator has internal load capacitors to reduce components. They are selected by firmware.

- The RTC oscillator frequency can be tuned using the CLKOUT or 32KHZ_CLKOUT output to measure the frequency.

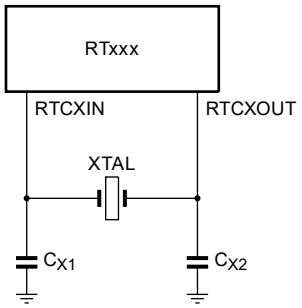


Figure 8. RTC oscillator

5.7 CLKIN input clock

The CLKIN input is available as a shared function on one of four GPIO pins on the i.MX RT500, see Figure 9. The system oscillator bypass bits select the main crystal oscillator or the CLKIN input as the source for the oscillator clock, shown as osc_clk in Figure 9.

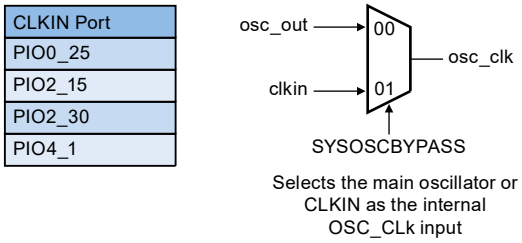


Figure 9. osc_clk input

The clock waveform must be a Complementary Metal-Oxide-Semiconductor (CMOS) 1.8 V rail-to-rail square wave. The maximum input frequency is 50 MHz due to pin loading. Configure CLKIN function using the appropriate FSEL field setting in the GPIO IOPCTL register. Select CLKIN by setting the SEL field to 0b001 in SYSOSCBYPASS.

The CLKIN function is configured in the GPIO pad control register and selected as the osc_clk with the system oscillator bypass bits.

5.8 CLKOUT output clock

The CLKOUT output is available as a shared function on one of five GPIO pins on the i.MX RT500, see Figure 10.

The CLKOUT output can be used as a dedicated clock output to other devices, with a wide range of source clocks and divisors as highlighted on the left side in Figure 10.

This clock output is very useful during system development to verify the frequency of the internal system clocks and to tune the crystal oscillators, whether they use internal or external load capacitors. The output can be disabled for production.

Note: *The CLKOUT function is shared on GPIO pins which may have more loading than dedicated outputs. Therefore, the waveshape may be attenuated or deformed at high frequencies but is sufficient for external frequency measurements.*

Note: *Higher frequency clocks may show wave deformation due to loading and drive strength. Full drive strength can be enabled to resolve it.*

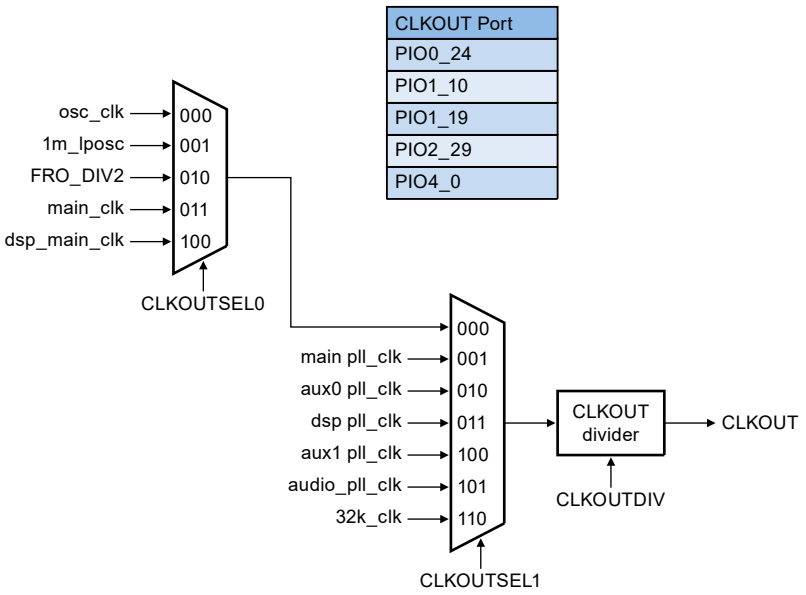


Figure 10. CLKOUT port

5.9 Oscillator load capacitance

Choosing load capacitor values for a crystal oscillator is a topic that can take more time to discuss and also to understand. First, let us look at what load capacitance is.

The load capacitance (also called C_L) of a crystal is different from the load capacitor values placed on the crystal pins (also called C_x and C_y). The crystal load capacitance is a crystal parameter used by the vendor to manufacture and test each crystal.

Crystal vendors generally specify a range of C_L values in their data sheets as manufacturing and test conditions. For example, 32.768 kHz crystal data sheet C_L values can range from 9 pF to 12.5 pF. A customer can choose the desired value. It is the responsibility of the customer to tune the crystal in their circuit. You must know the crystal C_L value in order to begin tuning.

Load capacitors C_x and C_y are placed from the crystal legs to the ground. While it may look like these caps are in parallel, they are actually in series across the crystal, see Figure 11.

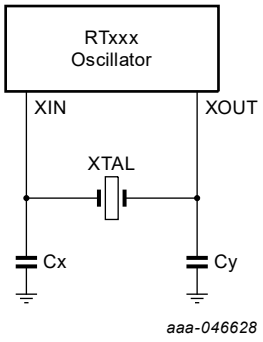


Figure 11. Load capacitance

There are many methods to calculate load capacitance, but none are accurate. At best, they are approximations.

We recommend using a simple calculation to determine the initial values of the external load capacitors. Then, after placing these values on the crystal, measure the frequency with a CLKOUT pin. The load capacitors can be increased if the frequency is higher than expected or decreased if the frequency is lower than expected.

Definitions:

- C_L - load capacitance of the crystal
- C_x, C_y - value of the load capacitors on the crystal pins
- C_{Pin} - approximate pad capacitance of each crystal pin
- C_{Stray} - stray board capacitance

Load capacitance expression:

1. $C_x = C_y \approx 2C_L – C_{Pin} – 2C_{Stray}$
   Or
2. $C_x = C_y \approx 2(C_L – C_{Stray}) – C_{Pin}$

Note: *It is an approximation.*

Example 1: Typical 32.768 kHz crystal:

$C_L = 12.5$ pF

$C_{Pin} = 3$ pF

$C_{Stray} = 0$ (ignore for first pass calculation)

$C_x = C_y \approx 2(12.5\text{ pF} – 0\text{ pF}) – 3\text{ pF} = 22$ pF

Example 2: Small 32.768 kHz crystal:

$C_L = 9$ pF

$C_{Pin} = 3$ pF

$C_{Stray} = 0$ (ignore for first pass calculation)

$C_x = C_y \approx 2\ (9\text{ pF} – 0\text{ pF}) – 3\text{ pF} = 15$ pF

Here are the definitions of the symbols used in the model and the simple calculation:

- C_L is the load capacitance of the crystal that you received from the vendor.
- C_x and C_y are the physical load capacitors placed on the crystal pins.
- C_{Pin} is an approximate pad capacitance of each oscillator terminal, also called the crystal pin of the MCU.
- C_{Stray} is the crystal industry term for the unknown board capacitance.
  The load capacitance expression is derived from a standard crystal industry formula, which involves C_L and the unknown C_{Stray} parameters.
  Note: *The derived expression is an approximation. As a matter of fact, the industry formula and other load capacitance calculations are also approximations, because there are other dependencies that cannot be defined in simple models.*

Refer to Load capacitance expression 1: Let C_x and C_y be the same value. Multiply the crystal load capacitance C_L by 2, subtract the pad capacitance, and then subtract 2 x stray capacitance.

The expression can be stated a second way as in Load capacitance expression 2. In the Example 1, we use a 32.768 kHz crystal with a C_L of 12.5 pF, the chip's pad capacitance of 3 pF, and ignore the stray capacitance effect for the first pass calculation. We see that the C_x and C_y load caps should each be about 22 pF. Use this value for the load caps and measure the frequency. This value is probably high because we disregarded stray capacitance, so we see the improvement using smaller values. Iterate with capacitors as necessary to get the frequency tolerance you desire.

Example 2 shows the first pass approximation for a crystal with a 9 pF C_L.

The C_{Pin} can range from 3 pF to 8 pF or more depending on the chip's package size. Smaller packages generally have lower pin capacitance.

The C_{Stray} depends on the PCB layout and board parameters. It can be measured on the PCB, but this does not necessarily mean that the crystal sees the same value because the measurement is done only from pin to ground and does not include other dependencies. The crystal industry suggests assigning an arbitrary value of 3 pF to 5 pF to this parameter.

Given the C_{pin} range information and C_{Stray} arbitrary values, we see that calculating load capacitor values with absolute accuracy is futile.

NXP recommendation (to approximate the initial load capacitor values and measure the resulting frequency) eliminates many guesswork and tedious capacitance measurements. So, calculate the approximate maximum load capacitance values with this relation, choose the closest standard capacitor values, measure the resulting `CLKOUT` frequency, then adjust C_x and C_y equally until the desired frequency accuracy is attained.

Due to differences and tolerances in the components involved, it is recommended to characterize multiple board and units (mainly MCUs and crystals) with the chosen C_x and C_y to get a distribution for the accuracies over a population. The CLKOUT function makes it easier and more accurate than measuring crystal signals.

Two more examples using different 24 MHz C_L values Example 3 and Example 4. In Example 3, the larger crystals have higher C_L values. A typical 24 MHz crystal has a load capacitance of 18 pF. Example 3 shows that the initial value of the load capacitors should be 33 pF.

Attach these to the crystal and measure the resulting frequency on the enabled `CLKOUT` pin.

- The frequency probably may be lower than 24 MHz.
- Decrease the capacitor values until the desired accuracy is attained.
- A smaller 24 MHz crystal package has a lower C_L value.

For more details, see Example 3 and Example 4 for the calculation these crystals.

Example 3: Typical 24 MHz crystal:

C_L = 18 pF

C_{Pin} = 3 pF

C_{Stray} = 0 (ignore for first pass calculation)

$C_x = C_y \approx 2(18\ pF - 0\ pF) - 3\ pF = 33\ pF$

Example 4: Small 24 MHz crystal:

$C_L = 10\ pF$

$C_{Pin} = 3\ pF$

$C_{Stray} = 0$ (ignore for first pass calculation)

$C_x = C_y \approx 2(10\ pF - 0\ pF) - 3\ pF = 17\ pF$

6 DEBUG, TRACE, JTAG SCAN, and PROGRAMMING

This section provides information about the debugging and programming features of the i.MX RT500.

6.1 Serial Wire Debug (SWD) mode

The i.MX RT500 uses SWD mode to support debugging of the Arm Cortex-M33 processor and Fusion DSP. The i.MX RT500 SWD signals are multiplexed on several GPIO pins. The clock and data signals are initialized as SWD functions by default on reset.

The clock signal is enabled as an input reset.

CAUTION: *Use at least 10 Kohm as an external register, but 100 Kohm pull-xxxx is recommended for the safety of the board.*

For more details, see Table 9.

The optional Serial Wire Output (SWO) provides data from the Instrumentation Trace Macrocell to improve debugging support.

The MIMXRT595-EVK board has an LPC4322-based Link2 debugger to save costs for users. It provides a USB debug connection to the MCU's SWD interface.

Table 9. SWD debug

GPIO / Signal	Description	Recommendation
PIO2_25 / SWCLK	Serial Wire Clock (SWC) input from the debugger. Internal weak pull-down at reset.	Add an external 100 Kohm pull-down.
PIO2_26 / SWDIO	Bidirectional SWD Data I/O. Internal weak pull-up at reset.	Add an external 100 Kohm pull-up.
PIO2_24 or PIO2_31 / SWO	Serial Wire Output (SWO) optionally provides data from the ITM for an external debug tool to evaluate.	Must be selected as a function before use.

6.2 Trace signals

Trace Port Interface Unit (PIU) connections are available on the i.MX RT500, see Table 10. The high-speed TRACE clock and data pins are multiplexed with GPIO pins.

Table 10. Trace signals

Signal	I/O	GPIO	Description
TRACECLK	Out	PIO0_21 or PIO4_23	Trace Clock
TRACEDATA0	Out	PIO0_22 or PIO4_24	Trace Data 0
TRACEDATA1	Out	PIO0_23 or PIO4_25	Trace Data 1
TRACEDATA2	Out	PIO0_24 or PIO4_26	Trace Data 2
TRACEDATA3	Out	PIO0_25 or PIO4_27	Trace Data 3

6.3 JTAG boundary scan

The JTAG is disabled on the initial reset and the Boot ROM checks if it is for debug access and not disabled for security via the OTP settings. The JTAG signals are multiplexed with GPIO pins that are Hi-Z in reset, see Table 11. JTAG boundary scan is available on the i.MX RT500. JTAG mode entry takes place during reset with a specific sequence, see Section "Enabling the TAP controller" of *i.MX RT500 Low-Power Crossover Processor Reference Manual with Addendum* (document IMXRT500RM).

Note: *JTAG is not used for debugging, but it is used only for boundary scan.*

Table 11. JTAG boundary scan

Signal	I/O	GPIO	Description
TCK	In	PIO0_8	JTAG Test Clock: This pin is the clock for the JTAG boundary scan when the JTAG mode is active. Input buffer is enabled in boundary scan mode.
TMS	In	PIO0_9	JTAG Test Mode Select: The TMS pin selects the next state in the TAP state machine. This pin is used for JTAG boundary scan when the JTAG mode is active. This pin has an internal pull-up and input buffer enabled in boundary scan mode.
TDI	In	PIO0_10	JTAG Test Data In: It is the serial data input for the shift register. It is used for JTAG boundary scan when the JTAG mode is active. This pin has an internal pull-up and input buffer enabled in boundary scan mode.
TDO	Out	PIO0_11	JTAG Test Data Output: It is the serial data output from the shift register. Data is shifted out of the device on the negative edge of the TCK signal. This pin is used for JTAG boundary scan when the JTAG mode is active. Input buffer is enabled in boundary scan mode.
TRST_N	In	PIO0_7	JTAG Test Reset: The TRST_N pin can be used to reset the test logic within the debug logic. It is used for JTAG boundary scan when the JTAG mode is active. This pin has an internal pull-up and input buffer enabled in boundary scan mode.

6.4 Boot source from OTP `PRIMARY_BOOT_SRC` [3:0] bits

Once the reset completes, the Boot ROM checks the OTP bit settings first to determine the boot source. When performing any OTP read/write function, the `VDDCORE` voltage must be set to 1.0 Volts or higher when `LDO_ENABLE` is externally tied high or low, see Table 12.

If the boot source field is not programmed, the bootloader checks the status of three GPIO pins to determine where to boot from.

Table 12. Boot session

Boot mode	Field	Primary boot source. (a.k.a. master boot source)
ISP_PIN_BOOT	b'0000	ISP pins determine the boot source.
QSPI_BOOT	b'0001	Boot from Octal/Quad SPI flash device on FlexSPI0
SDHC0_BOOT	b'0010	Boot from eMMC device connected to SDHC0 port.
SDHC1_BOOT	b'0011	Boot from eMMC device connected to SDHC1 port.
SPI_SLV_BOOT	b'0100	Boot via SPI slave interface using master boot mode.
	b'0101	Reserved.
UART_BOOT	b'0110	Boot via UART interface using master boot mode.
SPI_FLASH_ BOOT	b'0111	Boot from 1-bit NOR flash via SPI interface. The SPI instance used is chosen by fuse word 0x60 bit 17 to bit 19, for more details, refer to the fuse map.
USB_HID_ISP	b'1000	Use the USB-HID interface to download the boot image into SRAM and boot.
ISP_FUSE_ BOOT	b'1001	Boot into ISP mode, fuse word 0x60 bit 4 to bit 6 decides which peripheral is used for ISP mode, more details, refer to the fuse map
	b'1010	Reserved.
	b'1011	Reserved.
FlexSPI_REC_ BOOT	b'1100	Boot from Octal/Quad SPI flash device on FlexSPI0; If an image is not found check recovery boot using SPI-flash device through FlexComm. The FlexComm instance used is chosen by fuse word 0x60 bit 17 to bit 19, For more details, refer to the fuse map.
SDHC0_REC_ BOOT	b'1101	Boot from SDHC0 port device. If an image is not found, check recovery boot using SPI-flash device through FlexComm. The FlexComm instance used is chosen by fuse word 0x60 bit 17 to bit 19, For more details, refer to the fuse map.
SDHC1_REC_ BOOT	b'1110	Boot from SDHC1 port device. If an image is not found, check recovery boot using SPI-flash device through FlexComm. The FlexComm instance used is chosen by fuse word 0x60 bit 17 to bit 19, For more details, refer to the fuse map.
	b'1111	Reserved

6.5 Boot source from `ISP_Pin` [2:0]

If OTP bits are not set, Boot ROM reads the 3 In-System Programming (ISP) pins to determine the boot source, from USB, external memories, or serial comm channels.

Table 13. Boot source

Boot mode	ISP2 pin PIO3_29	ISP1 pin PIO3_28	ISP0 pin PIO1_15	Description
Reserved	low	low	low	Reserved
Reserved	low	low	high	Reserved

Table 13. Boot source*...continued*

Boot mode	ISP2 pin PIO3_29	ISP1 pin PIO3_28	ISP0 pin PIO1_15	Description
USB HID ISP	low	high	low	Boot to ISP mode, using USB-HID class
FlexSPI Boot	low	high	high	Boot from QSPI/Octal Flash devices connected to the FlexSPI interface 0. The i.MX RT5xx finds a valid image in an external QSPI/Octal Flash device. If there is no valid image found, the i.MX RT5xx enters in recovery boot or ISP boot mode.
SDIO 0 (eMMC)	high	low	low	Boot from an eMMC device connected to SDIO 0 interface. The i.MX RT5xx finds a valid image in the eMMC device. If there is no valid image found, the i.MX RT5xx enters in the ISP boot mode based on the value of OTP DEFAULT_ISP_MODE bits (6:4, BOOT_CFG [0]).
Reserved	high	low	high	Reserved
Serial ISP (UART, I2C, SPI)	high	high	low	The Serial Interface (UART, I2C, SPI) is used to program OTP, external FLASH, or eMMC devices
Serial Download	high	high	high	Serial Master boot is used to download a boot image over the serial interface (SPI Slave or UART, I2C, USB-HID)

6.6 Physical ISP pins configuration on EVK board

Boot modes can be configured using the external boot configuration ISP switch SW7 on the MIMXRT595-EVK board. The SW7 switch is configured to serial ISP mode as shown in Figure 12. If serial ISP mode is implemented, weak pull-ups and strong pull-downs are recommended.

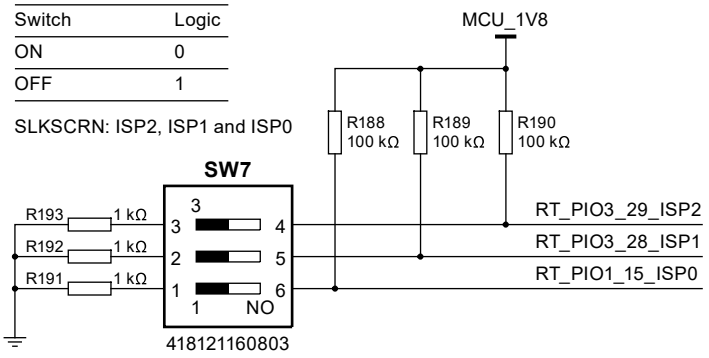


Figure 12. EVK ISP configuration

For more details, see Figure 13.

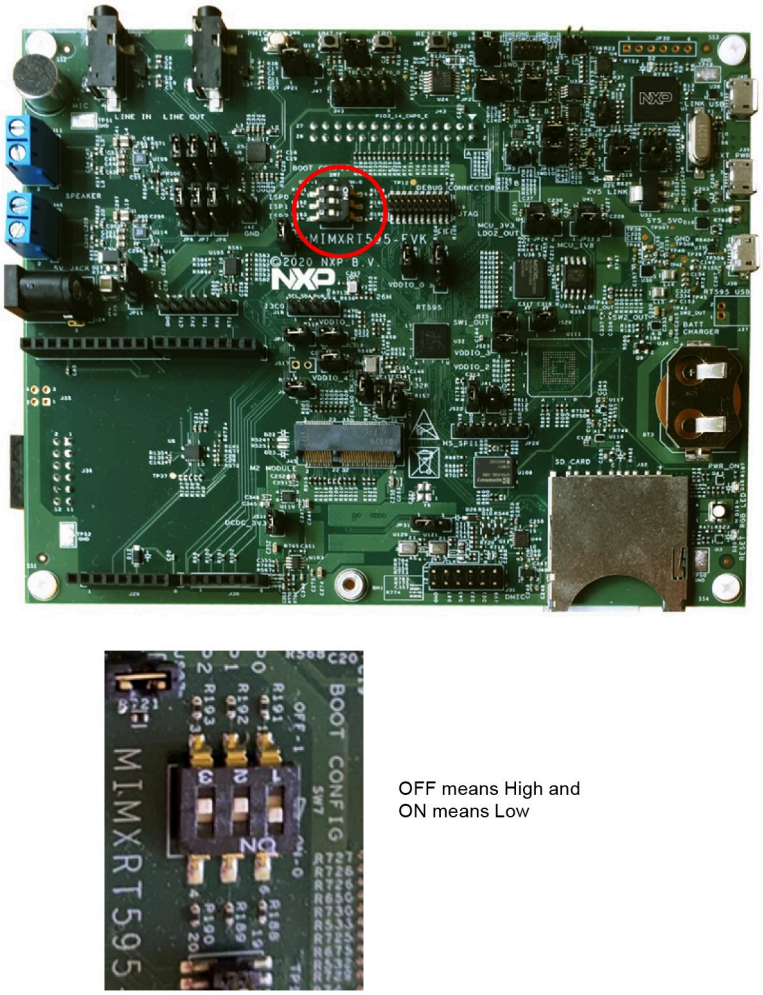


Figure 13. MIMXRT595-EVK board

6.7 Reset pin

The external reset pin is an active low input. A low resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. RESETN wakes up the part from deep power-down mode, see Table 14.

When used with a PMIC, tie this pin to the SYSRSTb pin or POWER_OK pin with a 100 Kohm external pull-up to VDD_AO1V8.

When used with the internal VDDCORE LDO enabled, this pin should have a 100 Kohm external pull-up to VDD_AO1V8. Add a 10 nF capacitor for debounce if used with a switch. This pin has an analog filter that suppresses glitches from 8 ns to 20 ns wide.

Table 14. Reset pin

Signal	Description	Recommendations
RESETN	External reset input: A low on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.	When used with a PMIC, tie this pin to the SYSRSTb or POWER_OK pin with a 100 Kohm external pull-up to VDD_AO1V8. When used with the internal VDDCORE LDO enabled, this pin should have a 100 Kohm external pull-up to VDD_AO1V8. Add a 10 nF capacitor for debounce if used with a switch. This pin has an analog filter that suppresses glitches from 8 ns to 20 ns wide.

7 Layout recommendations

This section provides the details about the layout of i.MX RT500.

7.1 Basic PCB design recommendations

The i.MX RT500 microcontroller is available in two small BGA packages.

- The 249 terminal Fan-Out Wafer-Level Package (FOWLP) package (7.0 mm x 7.0 mm x 0.725 mm, 0.4 mm pitch).
- The 141 terminal Wafer-Level Chip-Scale Package (WLCSP) package (4.525 mm x 4.525 mm x 0.49 mm, 0.35 mm pitch).

For other dimensions and detailed package information, see *i.MX RT500 Low-Power Crossover Processor Data Sheet with Addendum* (document IMXRT500EC).

High Density Interconnect (HDI) design methods are expected to be used with the 249 FOWLP and 141 WLCSP packages. The MIXMRT595-EVK board uses HDI techniques for the MCU (MIMXRT595SFFOC), as well as the PMIC (PCA9420UK), and audio amps (TFA9896UK) which are in narrow pitch BGA packages.

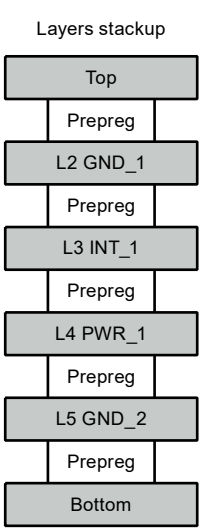
High-density interconnection methods include the use of smaller vias (microvias) that only connect two or three layers, unlike the through-hole vias of conventional PCB design. Conventional PCB design interconnection (through-hole vias) can be used with HDI.

7.2 Stack-up recommendations

High-speed design requires a proper PCB stack-up to ensure impedance control for critical interfaces and to minimize EMC effects. Impedance control depends on several factors, such as the trace width and space, associated dielectric and copper thicknesses, and required impedance. High-speed signals must have reference planes on an adjacent layer to provide constant impedance.

The recommended stack-up for each package is six or more layers, see Figure 14. The MIXMRT595-EVK uses six layers with the 7 mm square Fan-Out FOWLP package.

The total thickness: 1.6 mm +/- 10 %



Layer	Material	Thickness	Layer type	Dielectric constant	Loss tangent
Top	Copper	1 Oz	Routing		
Prepreg	TU-768	2.7 MIL	Thin dielectric	4	0.02
L2 Inner	Copper	1 Oz	Plane		
Prepreg	TU-768	4 MIL	Thin dielectric	4.2	0.02
L3 Inner	Copper	1 Oz	Routing		
Prepreg	TU-768	40 MIL	**Thick dielectric**	4.5	0.02
L4 Inner	Copper	1 Oz	Plane		
Prepreg	TU-768	4 MIL	Thin dielectric	4.2	0.02
L5 Inner	Copper	1 Oz	Plane		
Prepreg	TU-768	2.7 MIL	Thin dielectric	4	0.02
L6 Inner	Copper	1 Oz	Routing		

Figure 14. Layers stack-up

First, notice the dielectric thicknesses between the successive layers. L1 is tightly coupled to L2 with a 2.7 mil dielectric. L3 is tightly coupled to L2 with a 4 mil dielectric.

- L3 is isolated from L4 with a thick 40 mil dielectric.
- L4 is tightly coupled to L5 with a 4 mil dielectric.
- L6 is tightly coupled to L5 with a 2.7 mil dielectric.

The tight coupling of signals to planes with thin dielectrics is the basis of impedance control. The trace widths and spaces on the signal layers determine the desired signal impedance.

The recommended stack-up for each package is six or more layers. The MIXMRT595-EVK uses six layers for the 7 mm x 7 mm FOWLP package.

- L1 - Signals and components
- L2 - Ground plane
- L3 - Signals, power, and ground

Thick core:

- L4 - Power and ground
- L5 - Ground plane
- L6 - Signals, power, ground, and components

L2 and L5 are solid ground planes that provide the reference planes:

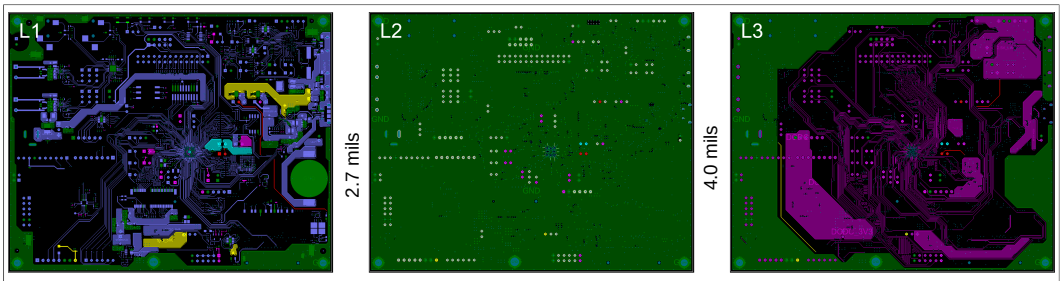
- L1 and L3 are tightly coupled to L2 as the reference plane
- L4 and L6 are tightly coupled to L5 as the reference plane

7.3 EVK Stack-up comments, top 3 Layers

Figure 15 demonstrates the coupling of the top 3 PCB layers.

Layers 1 and 3 are tightly coupled to the ground plane on layer 2.

- L1 - Contains signals and components, high-speed signal routing, and routed power traces.
- L2 - It is a solid ground plane that is a reference that provides the return paths for L1 and L3 signals.
- L3 - Contains high-speed signals, routed power, and ground.



L 1 - Signals and components
High-speed signal routing
Routed power

L2 - Solid ground plane
Reference for L 1 and L3

L3- Signals
High-speed signal routing
Routed power

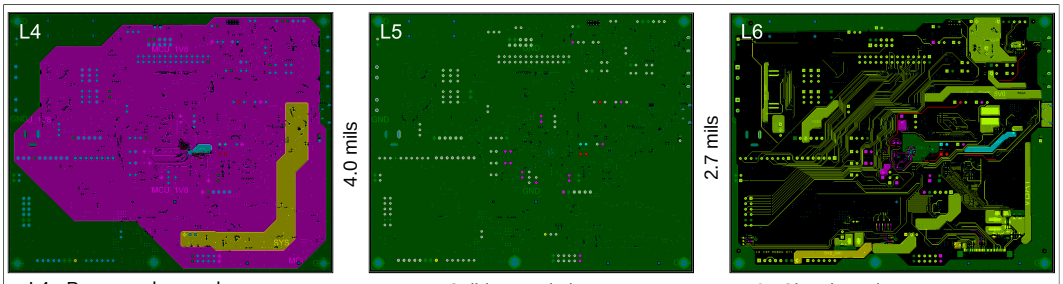
- L 1 signals are tightly coupled to L2 ground plane
- L3 signals are tightly coupled to L2 ground plane

Figure 15. Top 3 Layers of PCB

7.4 EVK stack-up comments, bottom 3 layers

Figure 16 demonstrates the coupling of the bottom 3 PCB layers. L4 and L6 are tightly coupled to the ground plane on L5.

- L4 - Contains the main power domains and ground.
- L5 - It is a solid ground plane that is a reference that provides the return paths for L6 signals.
  The thin dielectric between L4 and L5 creates board capacitance between the power domains and ground. This additional capacitance helps reduce the power domain impedance.
- L6 - Contains high-speed and low-speed signals, routed power, and components.



L4 - Power and ground

L5 - Solid ground plane
Reference for L4 and L6

L6 - Signals and components
Some high-speed routing
Routed power

- Power domains are tightly coupled to L5 ground plane.
- Plane on plane with thin dielectric creates capacitance to reduce power domain impedance.
- L6 signals are tightly coupled to L5 ground plane.

Figure 16. Bottom 3 layers of PCB

7.5 Trace impedance requirements

The trace impedance requirements for the MIMXRT595-EVK PCB were developed with the board vendor who provided guidance based on the signal impedance requirements.

- Except for critical impedance traces, we specified minimum trace widths of 4.0 mils and minimum spaces of 5.0 mils.
- For 50 ohm impedances, most single-ended high-speed traces with 4.5 mil widths over the 2.7 mil dielectric are used.
- For the USB 90 ohm differential impedance, 4.5 mil widths with 5 mil spaces over the 2.7 mil dielectric are used.
- The 100 ohm differential impedance for the `MIPI_DSI` signals uses 3.5 mil widths with 7 mil spaces.
- Additionally, the minimum via diameter of 8mils with an 18 mil pad is used for most high-speed signals.

MIMXRT595-EVK PCB requirements determined with board vendor, see Figure 17:

- Minimum trace width of 4.0mils and minimum space of 5.0 mils, except for certain critical impedance traces.
- 50 ohm impedance for most single-ended high-speed traces (use 4.5 mil widths over 2.7 mil dielectric).
- 90 ohm differential impedance for some differential pair traces, like USB (use 4.5 mil widths and 5 mil spaces).
- 100 ohm differential impedance for other differential pair traces, like MIPI_DSI (use 3.5 mil widths and 7 mil spaces).
- Dielectric thicknesses of 2.7 mils to 4.0 mils.
- Minimum via diameter of 8mils with 18 mils pad.

Layers	Single ended		Single ended		Differential			Differential			Differential		
	Trace width (Mils)	Impedance (Ohms)	Trace width (Mils)	Impedance (Ohms)	Trace width (Mils)	Trace spacing airgap (Mils)	Impedance (Ohms)	Trace width (Mils)	Trace spacing airgap (Mils)	Impedance (Ohms)	Trace width (Mils)	Trace spacing airgap (Mils)	Impedance (Ohms)
L1_TOP	4.5	50						4.5	5	90	3.5	7	100
L3 and L4	4.5	50						4.5	5	90	3.5	7	100
L6_BOTTOM	4.5	50						4.5	5	90	3.5	7	100

Figure 17. Trace impedance requirements

7.6 General high-speed routing recommendations

It is a general recommendation for high-speed routing, we may overstate the term high-speed routing, but it has been proven that when all signals are routed as high-speed signals, the system has better electrical and EMC performance.

High-speed signals (memory buses, serial interfaces, clock signals, and so on) must have defined return current paths (typically on an adjacent reference plane). Trace length and impedance control are required to achieve correct communication among high-speed devices, consider perfect eye diagrams for USB serial data. While low-speed signals do not necessarily require a reference plane to direct return currents, these signals can be affected by switching noise or radiating electromagnetic energy without a reference.

High-speed signals must not cross gaps in the reference plane. Gaps cause signal return discontinuities that cause reflections.

Avoid creating slots, voids, and splits into reference planes. It creates discontinuities that can degrade signal integrity and generate emissions. Review the via voids to ensure they do not create splits.

Provide ground return vias adjacent to signal vias when transitioning between different reference ground planes. This directs return currents between layers.

Use the area on the bottom layer directly underneath the Ball Grid Array (BGA) package to place the power supply bulk and decoupling capacitors.

7.7 HDI recommendations

The EVK six-layer implementation of HDI techniques uses microvias to connect the package balls on layer 1 to the ground on layer 2, and package balls on layer 1 to signals on layer 3. A thick core (40 mils of FR-4) separates the top 3 layers (referenced to layer 2) from the bottom 3 layers (referenced to layer 5).

Microvias are smaller than standard through-hole vias because they are only drilled through two or three closely spaced layers. (Recall the thin dielectric thicknesses between layers 1 and 2, and layers 2 and 3 in the stack-up above).

This HDI technique uses the via-in-pad process to enable efficient routing of BGA packages that have small ball pitches.

7.8 HDI recommendations, dimensions of microvias

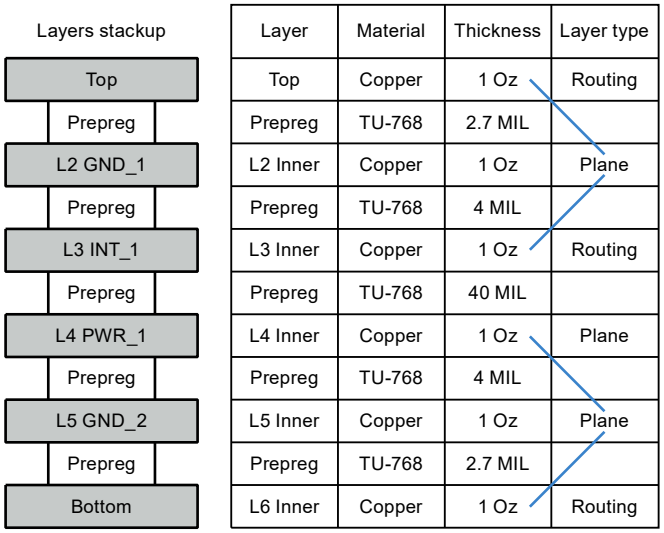
Following are the dimensions of the microvias used on the MIXMRT595-EVK board is:

- L1 to L2: 127 µm drill / 250 µm pad (5.0 mil drill / 9.8425 mil pad)
- L2 to L3: 127 µm drill / 250 µm pad
- L3 to L4: 150 µm drill / 400 µm pad (5.9055 mil drill / 15.7480 mil pad)
- L4 to L5: 127 µm drill / 250 µm pad
- L5 to L6: 127 µm drill / 250 µm pad

Note: *The L3 to L4 drill is larger since the L3 - L4 dielectric is thicker.*

As the minimum via dimensions are 8 mil drill with 18 mil pad for most signals. The microviases used on the MIXMRT595-EVK board are smaller than these:

The top 3 layers (L1 - L3) and the bottom 3 layers (L4 - L6) use 127 micron drills with 250 micron pads to connect between the 2 or 3 layers within each group. The corresponding dimension in mils is shown in Figure 18. The middle 2 layers (L3 - L4) have a thicker dielectric, so the drill size is increased to 150 microns with 400 micron pads.



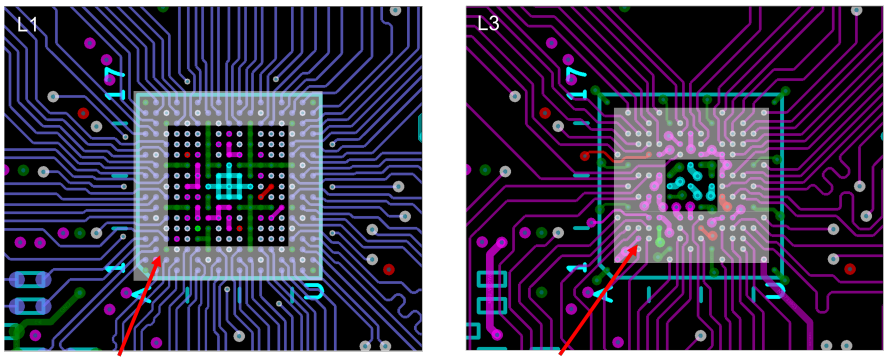
Layer	Material	Thickness	Layer type
Top	Copper	1 Oz	Routing
Prepreg	TU-768	2.7 MIL	
L2 Inner	Copper	1 Oz	Plane
Prepreg	TU-768	4 MIL	
L3 Inner	Copper	1 Oz	Routing
Prepreg	TU-768	40 MIL	
L4 Inner	Copper	1 Oz	Plane
Prepreg	TU-768	4 MIL	
L5 Inner	Copper	1 Oz	Plane
Prepreg	TU-768	2.7 MIL	
L6 Inner	Copper	1 Oz	Routing

Figure 18. Dimensions of microvias

7.9 HDI escape routing

HDI trace spacing is reduced to allow the escape routing of interior signals through the narrow pin (ball) pitches. Since all balls are routed on three layers (top, L2, and L3), only the top layer and L3 require smaller trace and space dimensions under the package. The outside ring of balls is routed on the top layer. These signals may later connect to other layers, but the escape route is the top layer.

The inside ring of balls is routed on L3 to take advantage of the L2 ground plane. The L1 to L3 transitions use via-in-pad microvias.



"Outside ring" signals from MCU begin routing on top layer.

"Inside ring" signals from MCU begin routing on L3 from via-in-pad microvias on L 1.

Figure 19. HDI escape routing

7.10 HDI recommendations, layers 1 - layers 3

In general, 2 common power balls on the package are routed to one microvia on the top layer as shown at the bottom of the left figure. Some microvias connect to 3 or 4 common power balls. These are on supplies that have multiple capacitors, like the `VDD1V8`, `VDDCORE`, `VDDIO_0`, and `VDDIO_1` supplies.

The 12 VDDCORE balls routed to 4 microvias are highlighted on the left figure. Microvias are used to connect layers 1-2, 2-3, 3-4, 4-5, and 5-6.

Skip vias are used to connect layers 1-3 and layers 4-6, as shown in the right figure.

Core vias between layers 3 and 4, as shown in Figure 20, are larger due to thicker L3 / L4 dielectric.

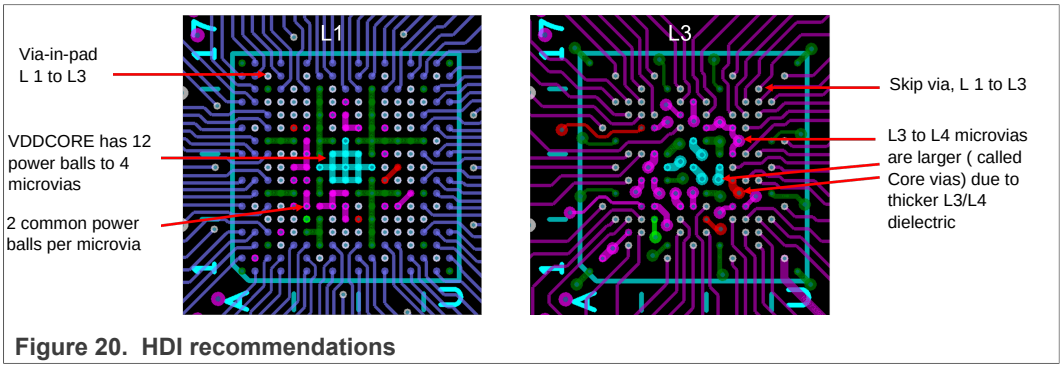


Figure 20. HDI recommendations

7.11 HDI recommendations, layers - 6

The capacitor quantities directly under the package (bottom layer L6) should generally be 1-per-via decoupling capacitors, plus one or two additional bulk capacitors. It reduces the number of capacitors from 1-per-pin to 1-per-2 or more pins on some supply domains.

However, when multiple balls share a via, larger decoupling capacitor values should be used. In this design, we use 0.22 µF ceramic bypass capacitors instead of the 0.1 µF capacitors normally used on conventional 1 capacitor-per-pin design.

Bulk and decoupling capacitors located directly underneath the MCU on the bottom layer.

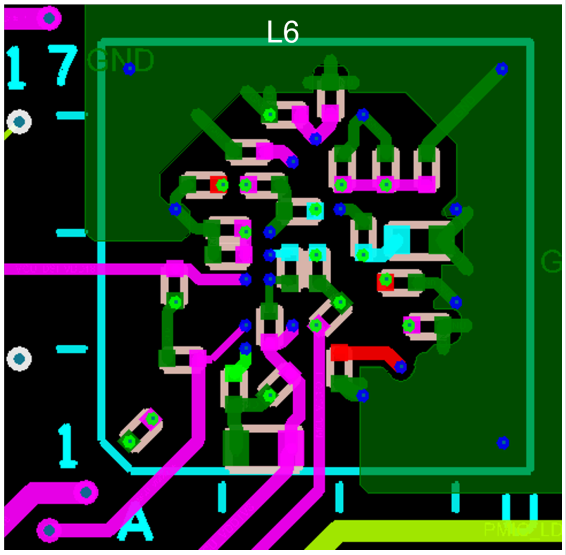


Figure 21. The bottom layer L6 of the PCB

7.12 HDI implementation

HDI implementation means that there may be a different number of vias from the top layer to the bottom layer.

Observe the progression from the top to the bottom layers, see Figure 22:

- Image A shows all the MCU ball pads on the top layer.
- Image B shows the corresponding via-in-pad microvias for the MCU on the top layer.
- Image C shows that many fewer microviases are connected to the decoupling capacitors on the bottom layer.

There are two reasons for it:

1. Many microviases on the top layer are signals that terminate on L3.
2. Some of the power supply microviases are tied together on intermediate layers.

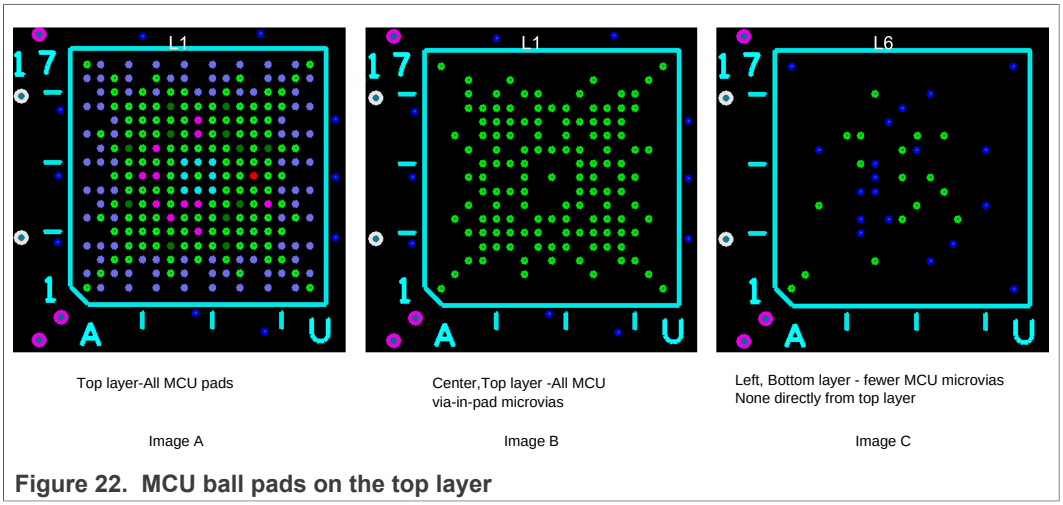


Figure 22. MCU ball pads on the top layer

7.13 Bulk and decoupling capacitor placement

All the high-speed BGA devices, like the MCU and memory, should have the small decoupling and larger bulk capacitors placed on the bottom side of the PCB, directly underneath the device. The 0201 decouplings and 0402 and 0603 bulk capacitors must be mounted as close to the power vias as possible. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current demand by the processor.

The following list provides the main recommendations to implement the correct decoupling scheme:

- Place the largest capacitance in the smallest package that the budget and manufacturing can support.
- For high speed bypassing, select the required capacitance with the smallest package (for example, 0.22 µF and package 0201).
- Minimize the trace length (inductance) to small caps, since series inductance cancels capacitance.
- Tie the capacitors to the GND plane directly with a via.
- Place the capacitors close to the power contact of the appropriate power domain.

7.14 Crystal oscillator PCB guidelines

This guidance is for crystal oscillator layouts. Locate crystals and components on the same layer as MCU. The crystal pins are normally placed along the edge of the package to allow same layer routing, which avoids discontinuities like vias. The adjacent layer should be a ground plane. It is always good guidance for digital and analog circuits.

Traces should be as short as possible and must not cross or couple with other signal lines. The crystal signal loop area must be made as small as possible to minimize the noise coupled through the PCB and to keep the parasitics as small as possible. It means to keep the traces as short as possible and on the same layer. The loop area is all the space between the 2 crystal traces. For more details, see Figure 23.

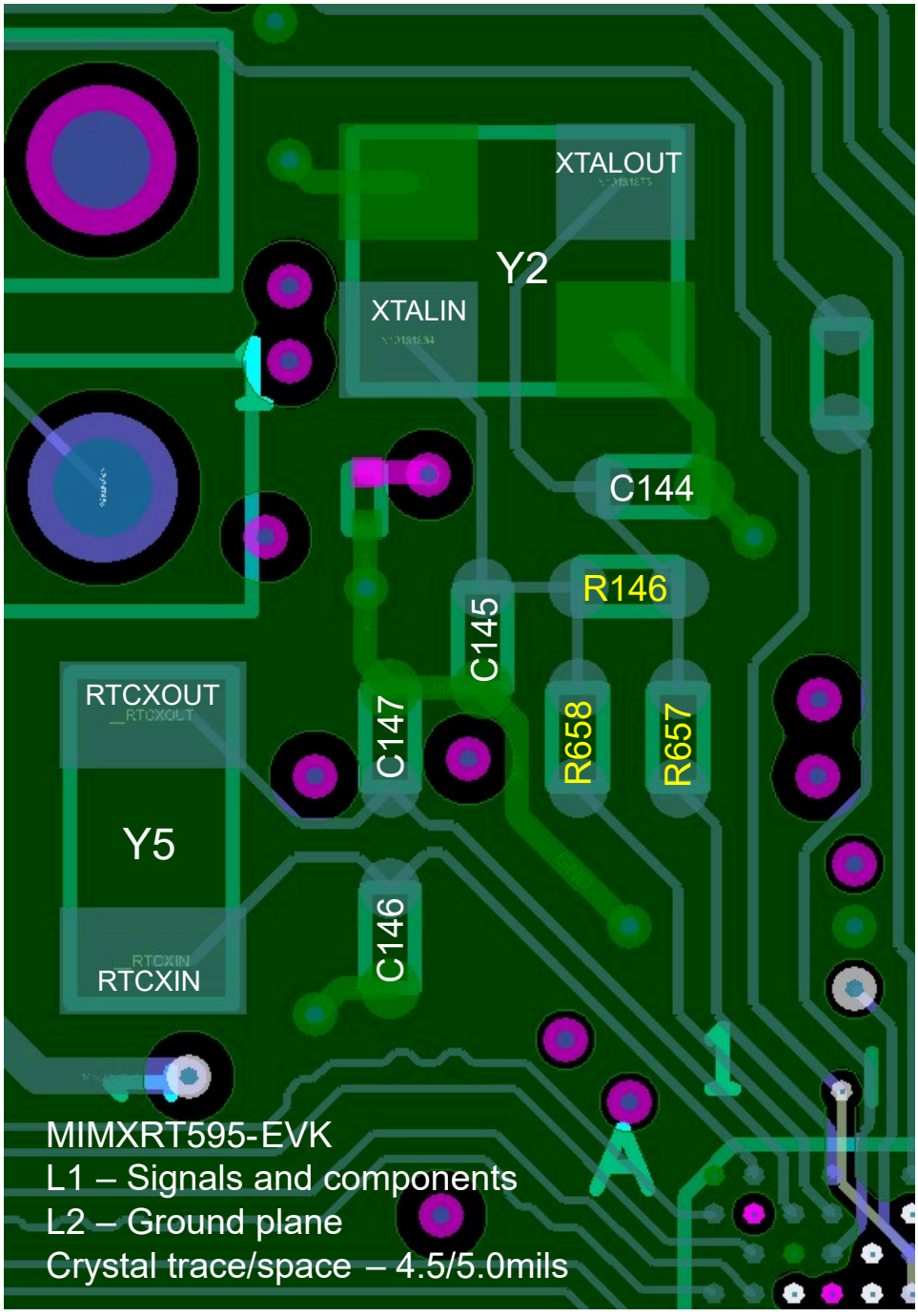


Figure 23. Crystal traces

We recommend placing load capacitors for the RTC oscillator even when using internal capacitors, in case the internal capacitors do not have enough tuning resolution. It is important to maintain the RTC frequency accurately.

Note: *Several resistors are highlighted in yellow in Figure 23. R146 is the main crystal oscillator feedback resistor, it is only required when the high gain mode is used.*

R657 is a small 22 ohm resistor used to limit current in the high gain mode. Series resistance is not needed for crystals above 8 MHz.

R658 is a shorting resistor, the only purpose of R658 is to be removed if an external oscillator is applied to that node. It is not recommended in any crystal application.

7.15 EVK memories octal flash (U38)

The EVK external memory schematics and layouts point out some good and poor design practices, see Figure 24 and Figure 25. Some good and poor design practices are described as follows:

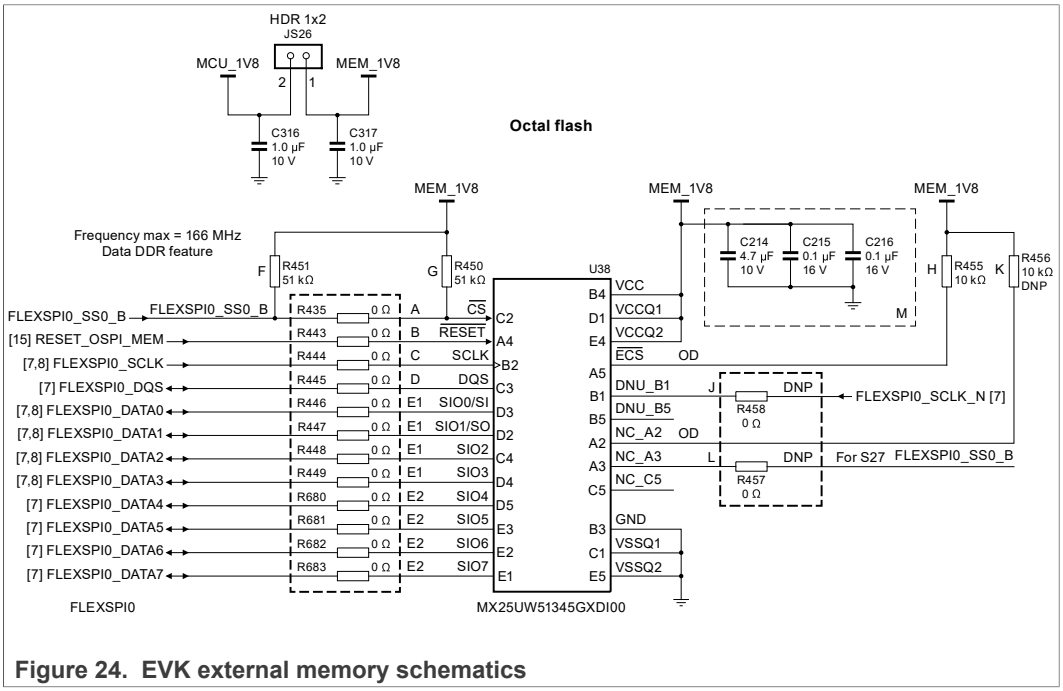


Figure 24. EVK external memory schematics

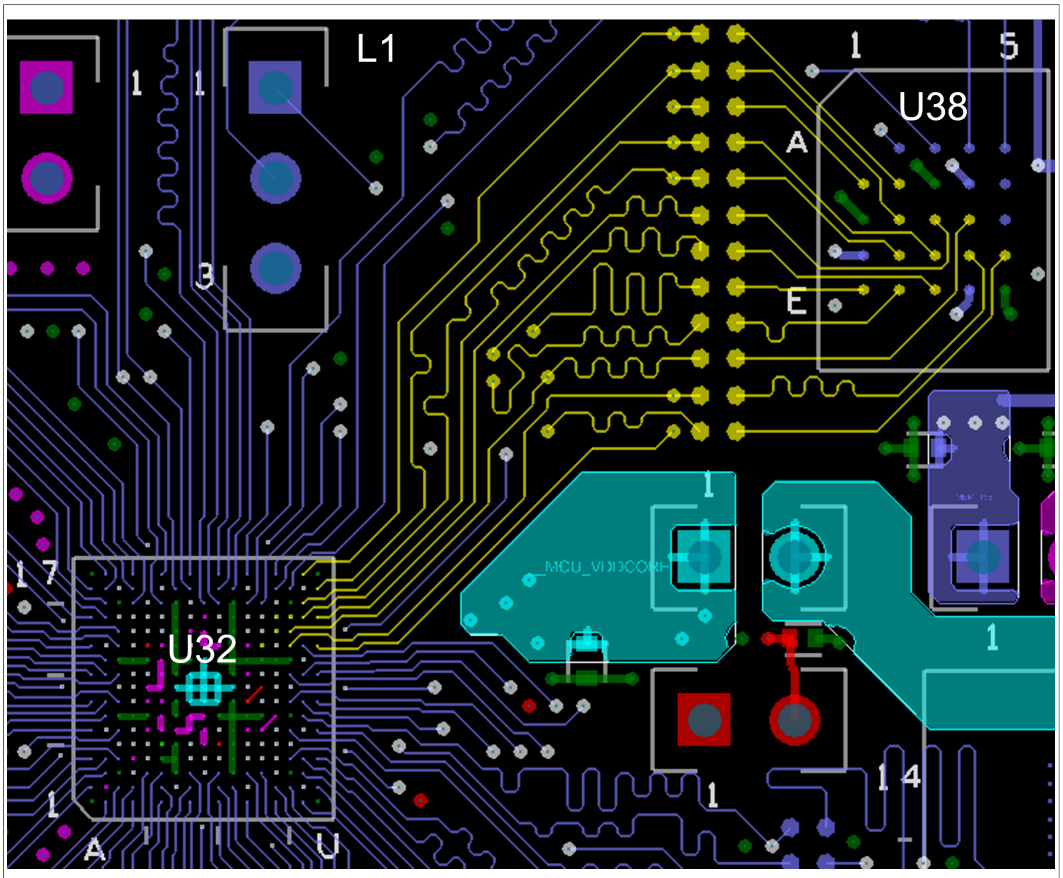


Figure 25. EVK external memory layouts

- Octal flash: Most data and control lines are routed on L1, it is good because all the HS signals between MCU and memory must be on the same layer. The MCU and memory can be on different layers, but all the HS signals should be on one layer.
- Matched signal lengths: It is good and required for high-speed bus signal integrity to match signal lengths, layer routing, and matched vias.
- L2 ground reference for impedance control: It is good since all the HS signals should have a ground plane for return currents.
- Several data lines are routed on L1 and L3: It is poor since all HS signals between MCU and memory should be on the same layer.
- Shorting resistors for shared components and signals: It is poor because these options create stubs and interfere with impedance control. However, these options are necessary to demonstrate the functionality of multiplexed functions on an evaluation board. Shorting resistors must be used in a development environment, not in production.

Note: *This interface uses the* `FLEXSPI0` *bus which is shared with the QSPI flash memory on the EVK.*

7.16 EVK memories QSPI flash (U37)

Continuing to look at good and poor design practices as fallows, for more details, see Figure 26 and Figure 27.

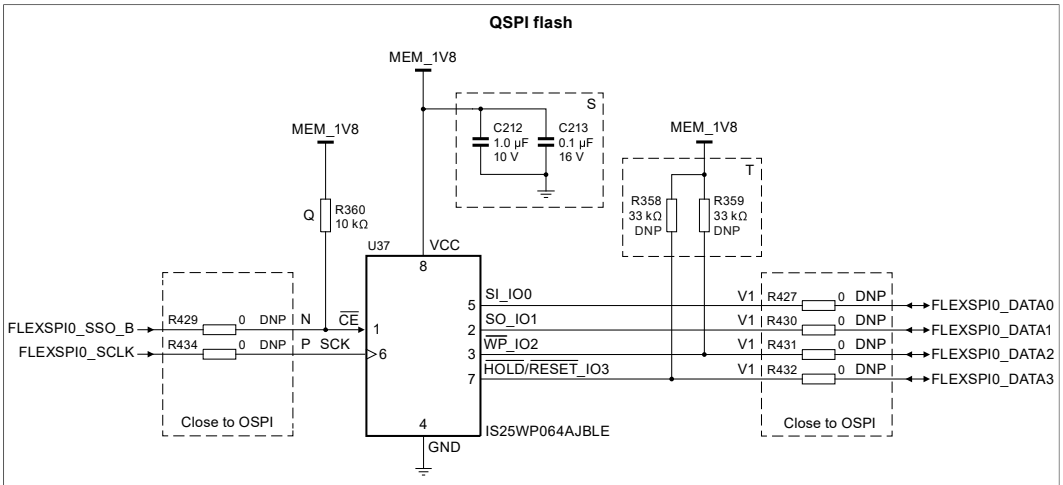


Figure 26. QSPI flash schematic

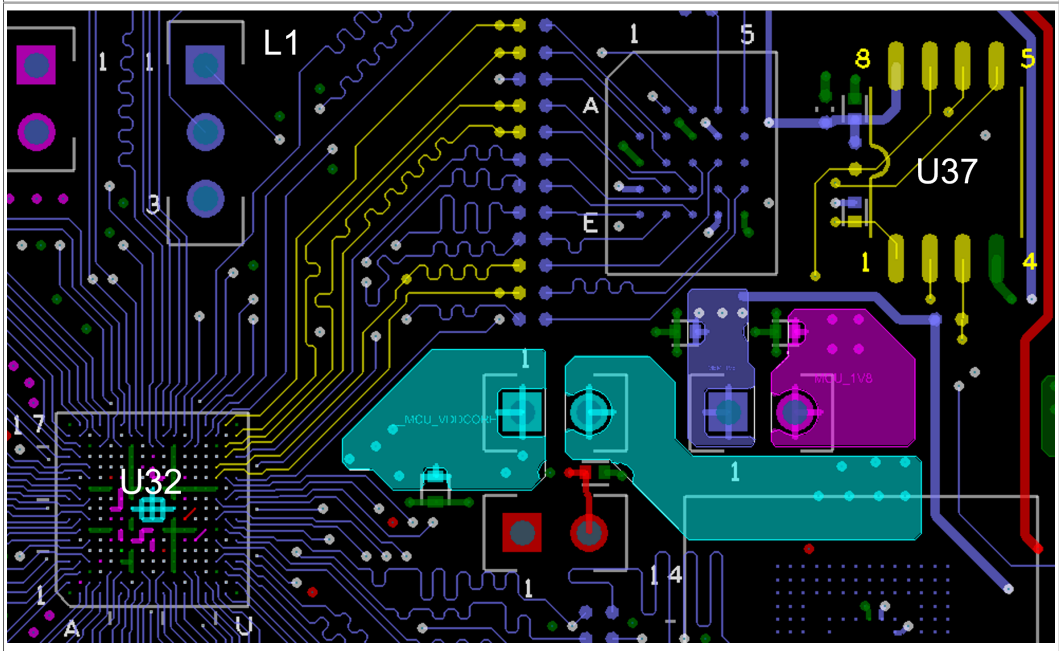


Figure 27. QSPI flash layout

- QSPI Flash, data, and control lines are shared on L1 and continue from resistors on L6: It is poor since all HS signals between MCU and memory should be on the same layer. The resistors create stubs that degrade signal integrity.
- Shorting resistors for shared components and signals: It is poor since these options create stubs and interfere with impedance control.

Again, these design choices are necessary to demonstrate functionality on an evaluation board. The memory interface works but is not guaranteed to have the best signal integrity. Worse, the stubs and layer transitions contribute to emissions. Do not copy for production.

Note: *This interface uses the* `FLEXSPI0` *bus which is shared with the Octal flash memory on the EVK.*

7.17 EVK memories PSRAM (U108)

Continuing to look at good and poor design practices as fallows, for more details, see Figure 28 and Figure 29.

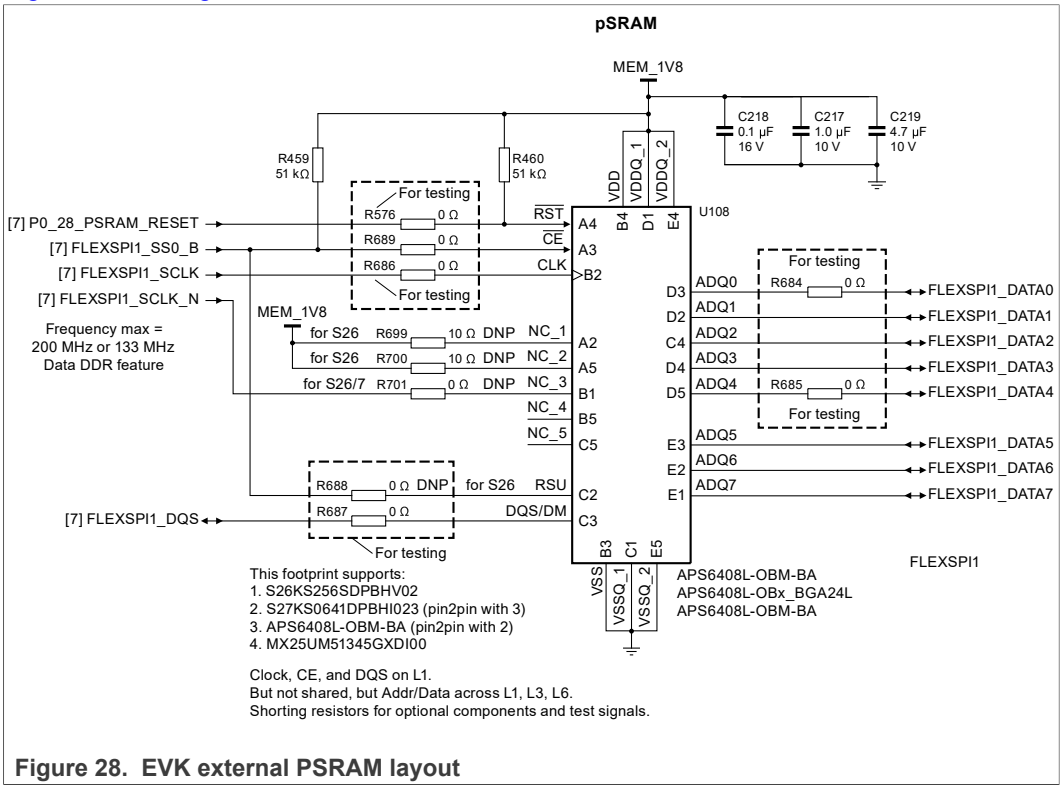


Figure 28. EVK external PSRAM layout

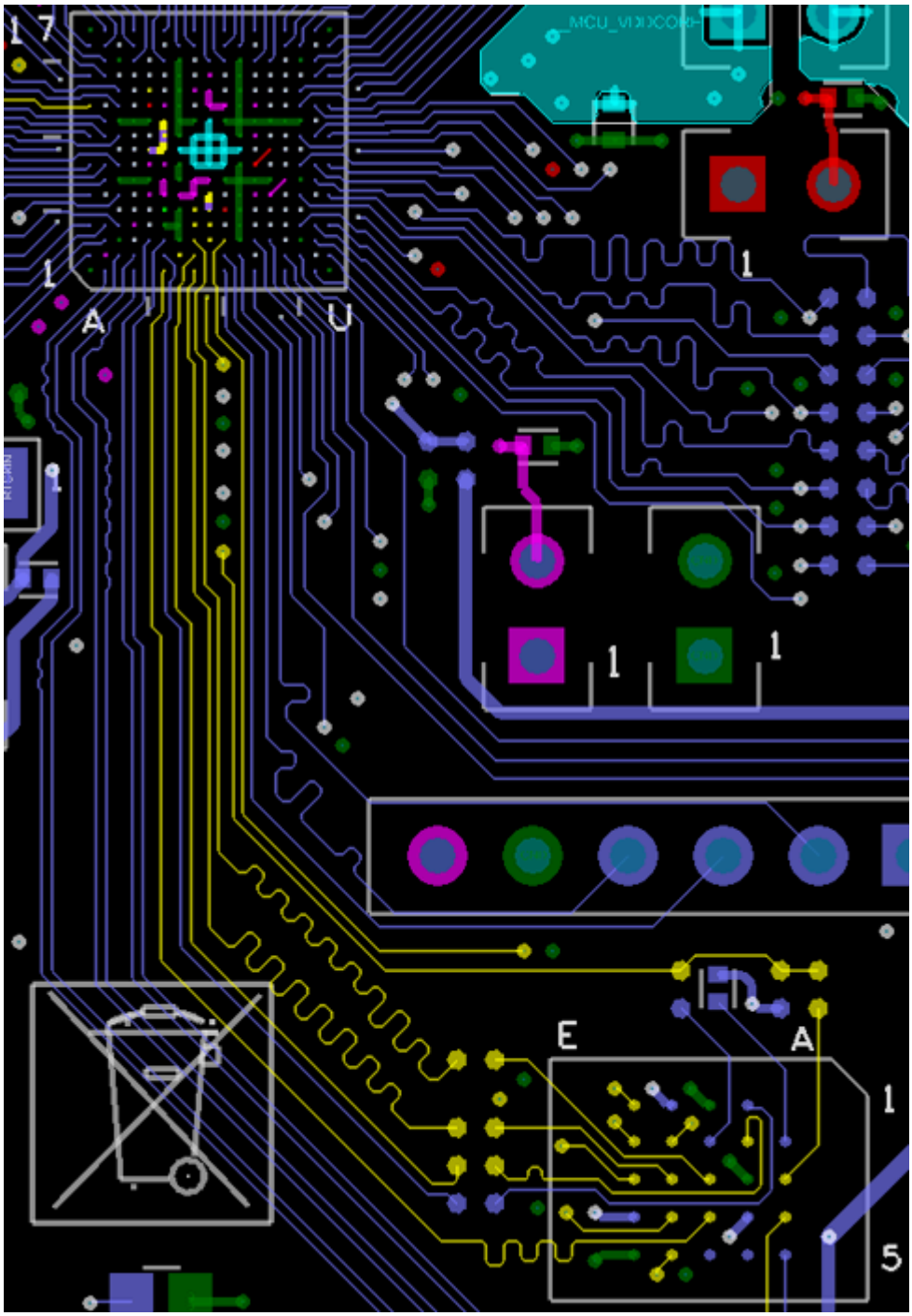


Figure 29. EVK external PSRAM layout

For the PSRAM footprint, a few lines are completely on the top layer.

- Addr/Data lines are routed across several layers: It is poor since all HS signals between MCU and memory should be on the same layer and have matched lengths for signal integrity.

- L2 ground reference: All HS signals should have a ground plane for return currents. L6 signals do not have the same reference as L1 signals. The MCU and memory can be on different layers, but all HS signals must be on one layer.
- Shorting resistors for optional components and test signals: It is poor since these options create stubs and interfere with impedance control.

Again, these design choices are necessary to demonstrate functionality on an evaluation board. Do not copy for production.

Note: *This interface uses the* `FLEXSPI1` *bus on the EVK.*

7.18 EVK memories eMMC (U111) and SD card

Continuing to look at good and poor design practices as fallows, for more details, see, Figure 30, Figure 31, and Figure 32.

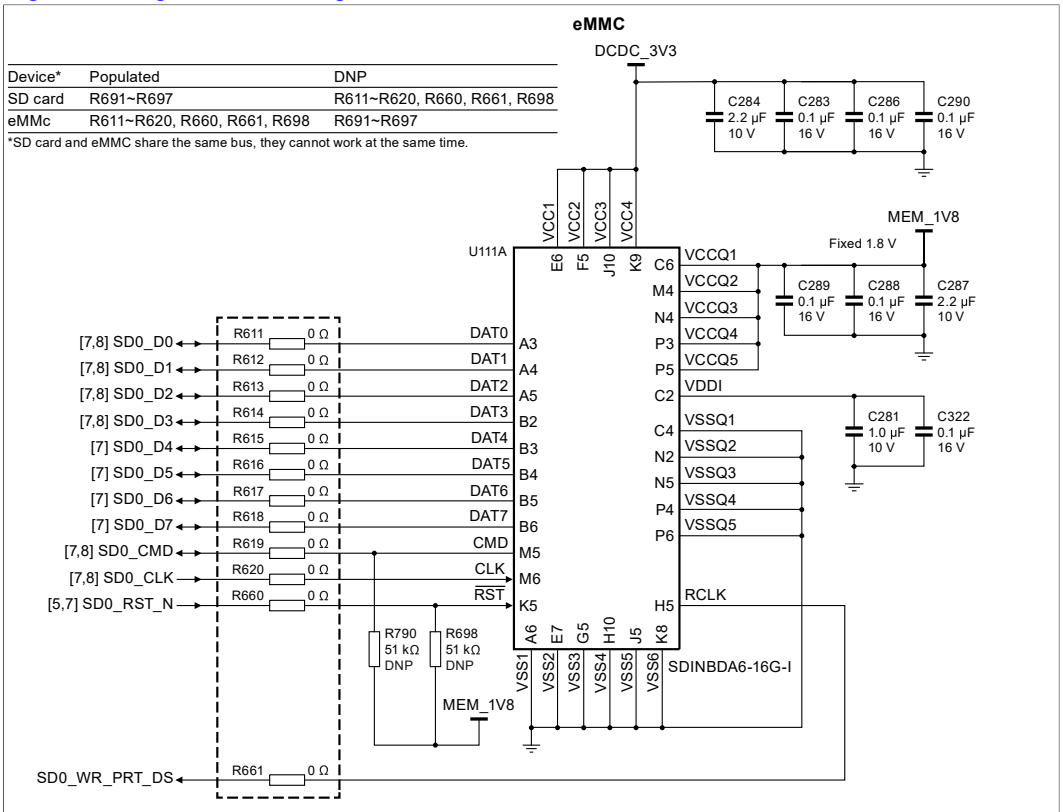


Figure 30. EVK external eMMC schematic

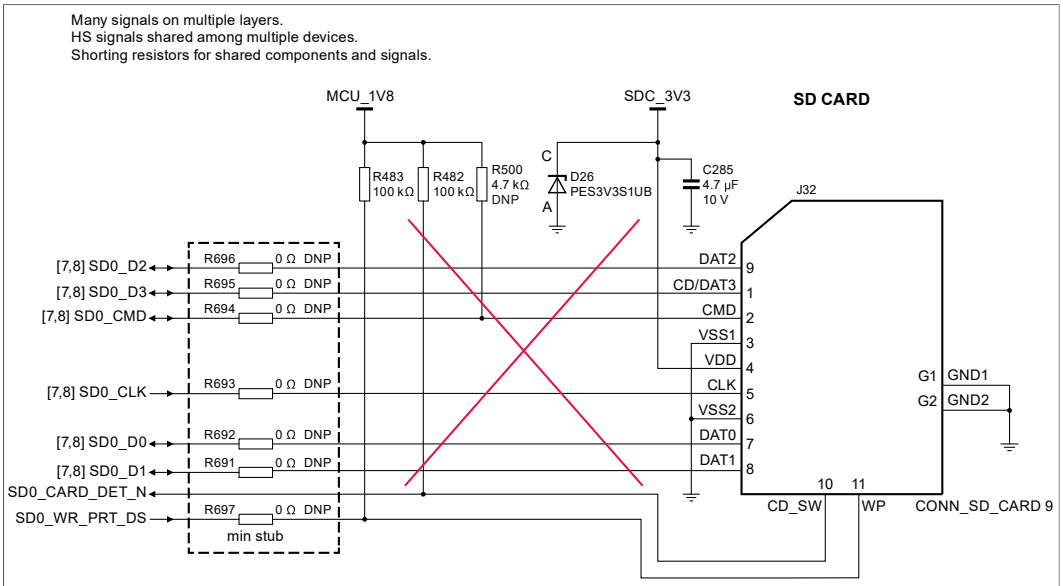


Figure 31. EVK SD card schematic

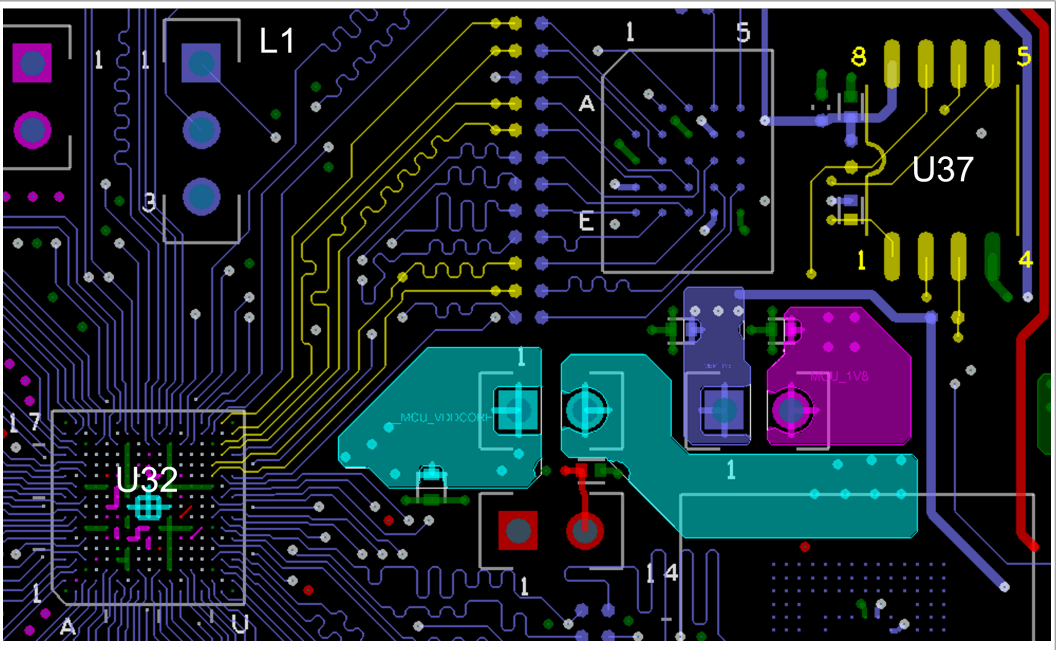


Figure 32. EVK external eMMC and SD card layout

- The eMMC and SD Card interface has many signals on multiple layers: It is poor since all HS signals between MCU and memory should be on the same layer.
- Shorting resistors for shared components and signals: It is poor since these options create stubs and interfere with impedance control.
- L2 ground reference: All HS signals should have a ground plane for return currents. L6 signals do not have same reference as L1 signals.

Again, these design choices are necessary to demonstrate functionality on an evaluation board. Do not copy for production.

This interface uses the SD0 bus on the EVK.

Due to the removal of 3.3 V support on the high-speed pads, the SD card interface is no longer supported. This considerably reduced the current leakage on VDD1V8. An erratum is issued to describe this further describe. We are evaluating the use of using an external level shifter to enable this.

Note: *The SDIO and MMC devices are unaffected.*

7.19 i.MX RT500 power domains

Here are some comments and cautions regarding jumpers on the evaluation board. Jumpers and 0 ohm resistors are used on the EVK to enable current measurements for various hardware and software configurations.

These must not be used in an end application because they require additional components and routing. Additional trace length is needed to place the jumper/resistor further from the target, it adds inductance to the power domain. Jumpers are tall structures that can radiate or couple external noises. This contributes to EMC emissions and susceptibility.

Note: *The evaluation boards are typically tested to Class A emissions levels which are looser than the Class B emissions levels for consumer goods.*

CAUTION: *If jumpers or 0 Ω resistors are used for multi-pin supplies, a bulk capacitor should be placed close to the jumper on the MCU side. This ensures the minimum bulk capacitance when the jumper or resistor is removed, and an external supply is attached to the node.*

The three jumpers shown in Figure 33 are for convenient attachment to an ammeter and have bulk capacitance on the MCU side. The 40 ohm resistors can be replaced with low-value resistors to perform differential voltage measurements to calculate the current.

Note: *These do not require bulk capacitance on the MCU side since the decoupling caps are located close to the MCU.*

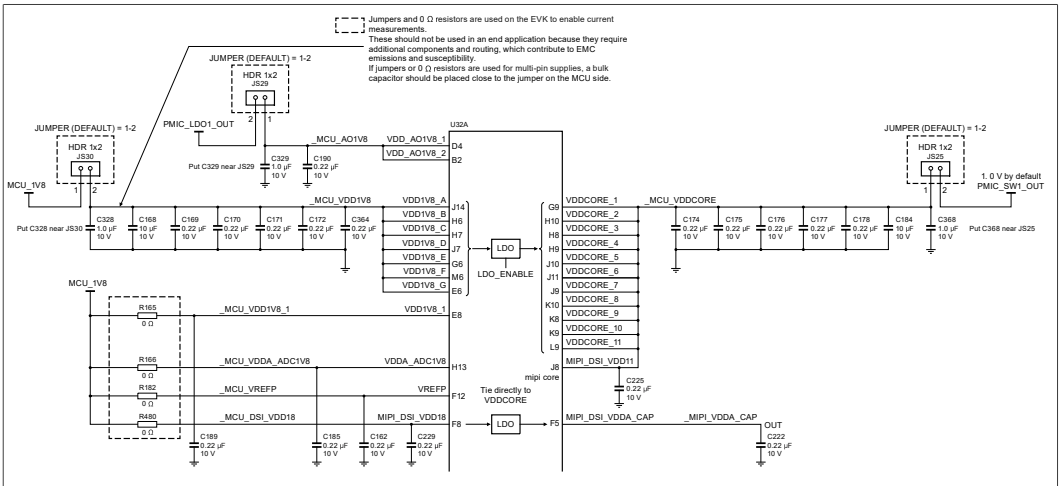


Figure 33. Evaluation board, schematic

Similar comments as before for the jumpers and 0 Ω resistors used for these power domains. In all cases, a bulk capacitor is placed on the MCU side of the jumper on supplies that have multiple pins.

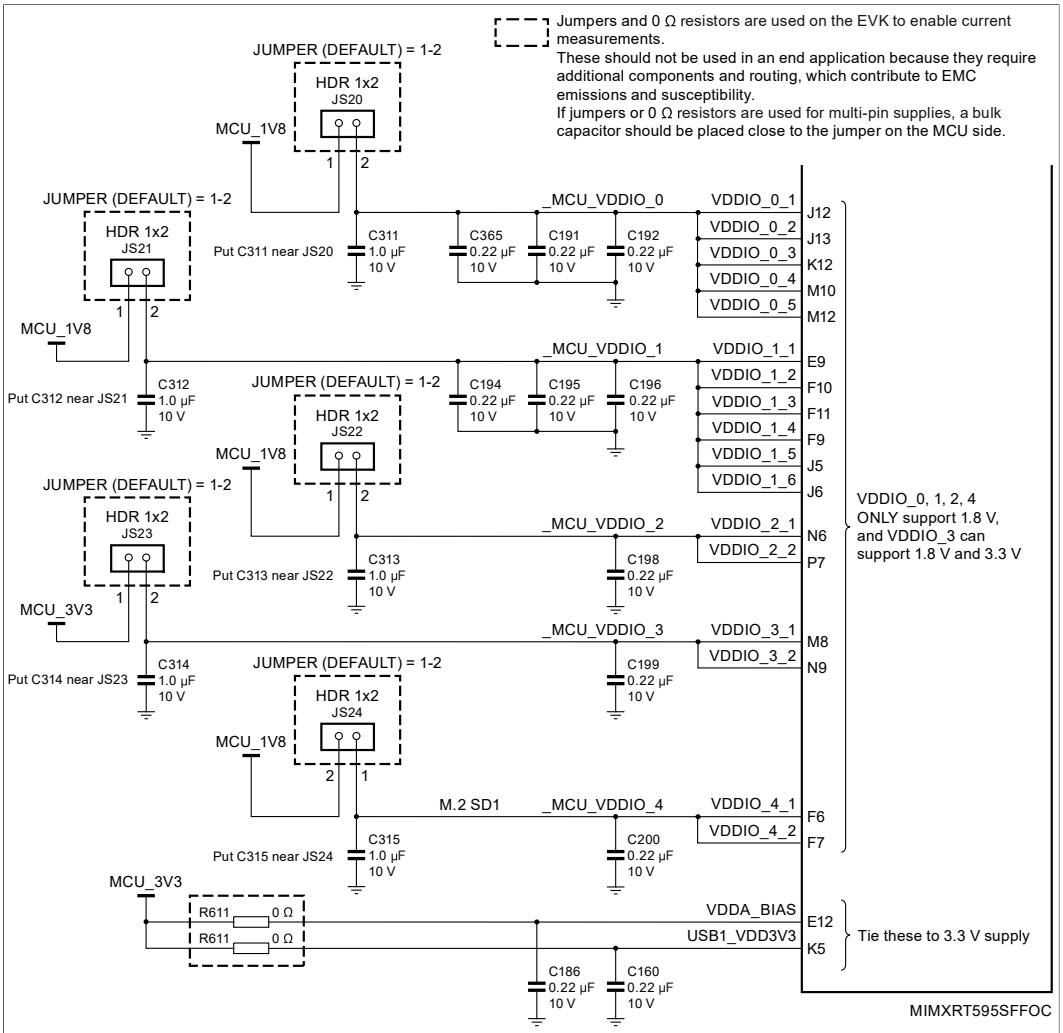


Figure 34. Schematic

7.20 MLCC capacitor DC bias effect

The Multi-layer Ceramic Capacitors (MLCCs) are beneficial since they miniaturize the size of the many ceramic capacitors required to adequately decouple power domains. However, MLCCs have one significant trade-off that must be addressed, the effect of DC bias:

- When DC voltage increases, then capacitance of a small package decreases sharply
- An MLCC may have less than 25 % of its rated capacitance at rated voltage

This can be critical for bulk capacitors on power domains if there is not enough charge to pass to the decoupling capacitors during signal switching, see Figure 35.

One rule of thumb is to choose 3 x DC voltage – however, this should be verified before the final component choice.

This example shows that the selected 2.2 µF capacitor rated at 6.3 V and in the 0402 package has less than 1 µF of capacitance at 3.3 V, and much less at 6.3 V. It can be good or bad depending on used case.

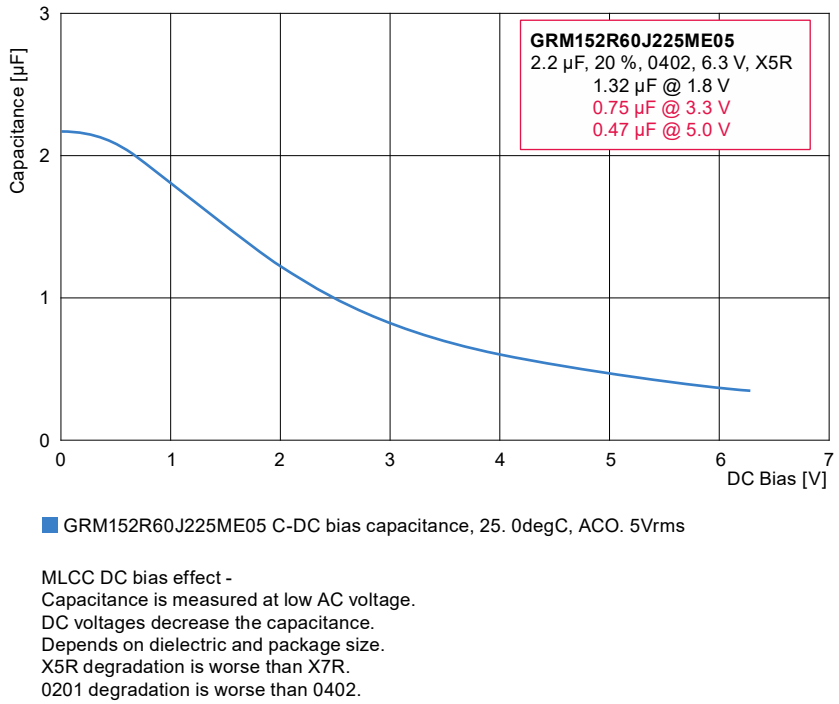


Figure 35. MLCC vendors supply capacitance vs DC bias curves

7.21 MLCC capacitor DC bias effect recommendations

The following are the recommendation for MLCC capacitor DC bias effect.

- The recommended 10 µF capacitor is the 0603 package, 16 V, 20 %, X5R, or X7R.
  - The 0805 package is acceptable.
- The recommended 1 µF capacitor is the 0402 package, 10 V, 10 %, X5R, or X7R.
- The recommended 0.22 µF capacitor is the 0201 package, 10 V, 20 %, X5R, or X7R.
- These part numbers were selected with the Murata SimSurfing tool. Other parts can be used.
  Note: *The MLCC thickness also affects DC bias characteristic.*

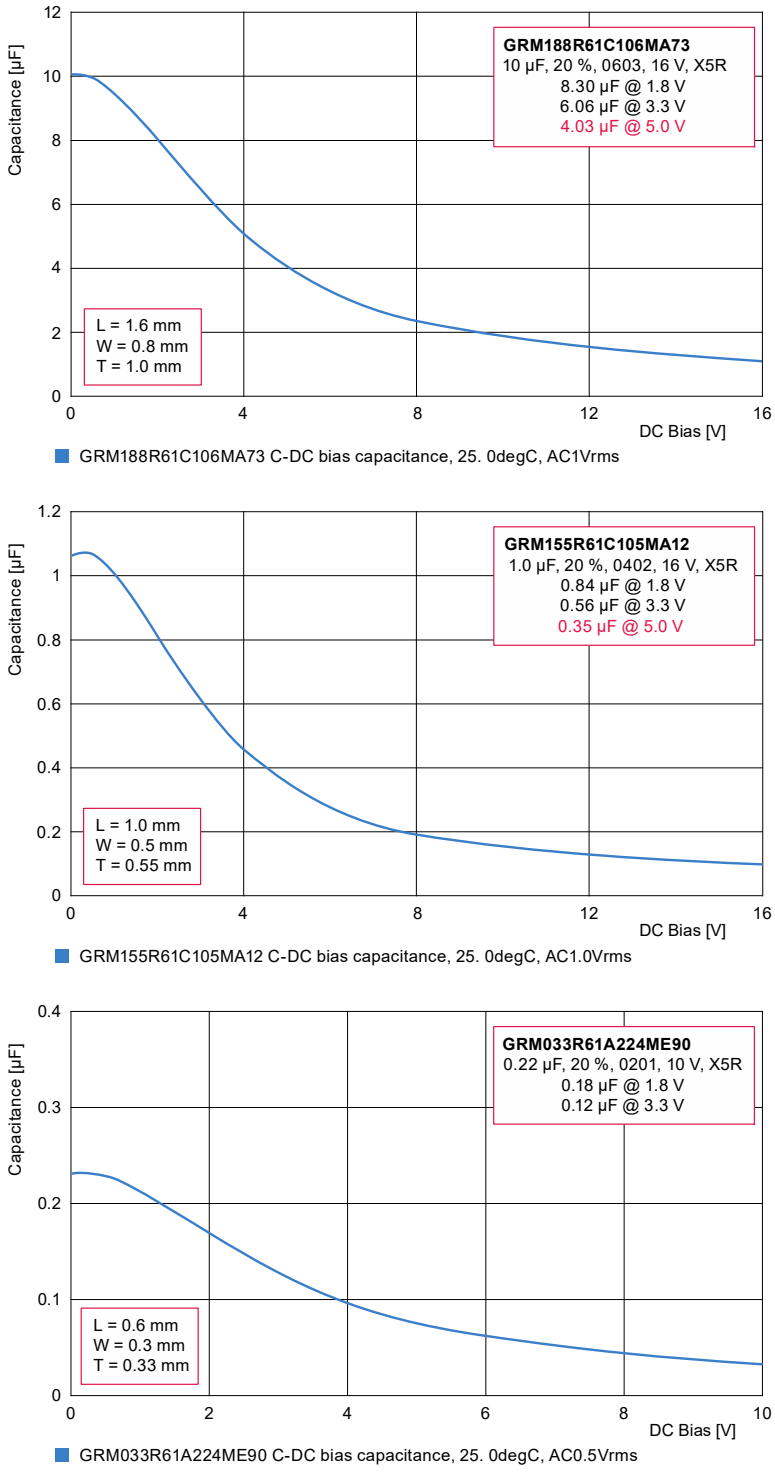


Figure 36. MLCC capacitor DC bias effect

8 Conclusion

Reviewed the multiple power domains on the chip, how to filter them, the power sequencing for these domains, and the implementation of the recommended PMIC for i.MX RT500 system power.

Examined the crystal oscillators that feed the internal clock systems, as well as the features of these oscillators. Also, reviewed the external clock input and clock output functions. Additionally, explained the crystal load capacitance and the recommendation to determine the proper load capacitor values.

The Debug, Trace, JTAG Scan, and In-System Programming connections were reviewed.

Layout requirements and recommendations were presented with examples from the i.MX RT500 EVK. General high-speed design and specific HDI design recommendations were discussed. Design trade-offs in the EVK were presented as a precaution before copying the exact circuits and layout for actual applications. Finally, we discussed the DC bias effect of MLCC capacitors and provided guidance for decoupling capacitor selection.

9 Revision history

Table 15 summarizes the changes done to this document since the initial release.

Revision history

Revision number	Date	Substantive changes
0	15 November 2022	Initial release

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